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# MS-7B18

## CFL Platform

ATX

Ver: 1.0

### CPU:

*Coffee lake S*

### System Chipset:

*Z390 PCH\_H*

### Onboard Chip:

*HD Audio Codec:ALC892*

*LAN-Intel I219*

*LAN-Intel I211*

*SIO:NTC6797*

*Flash ROM: SPI 128 MB X1*

### Main Memory:

*DDRIV (5000MHz) \* 4 (Dual Channel)*

### ACPI:

*LDO*

### PWM:

*IMVP8 -UPI9521*

### Expansion Slots:

*PCI Express (X16) Slot \* 1*

*PCI Express (X4) Slot \* 2*

*PCI Express (X1 ) Slot \* 2*

*M2 (X4 ) Slot \* 2*

### Other:

*SATA3.0 \*6*

*USB2.0 \*6*

*REAL USB3.1 Gen2 \*3+TYPEC\*1*

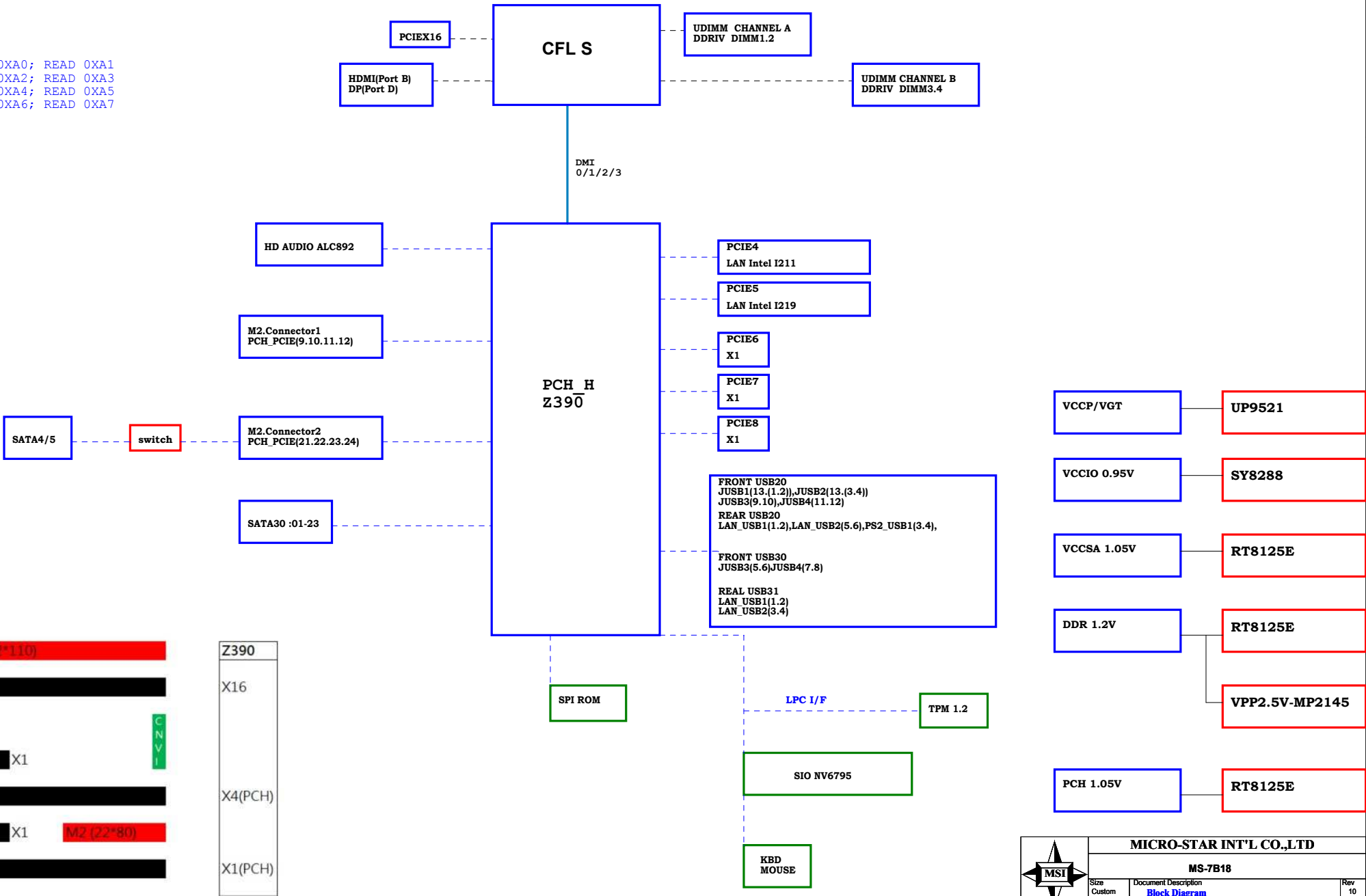
*FRONT USB3.1 Gen1 \*4*

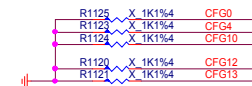
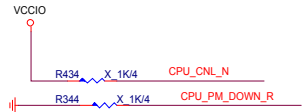
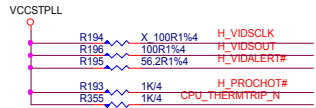


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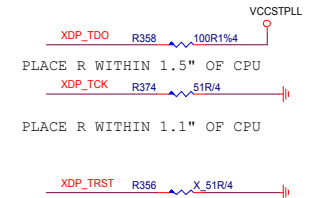
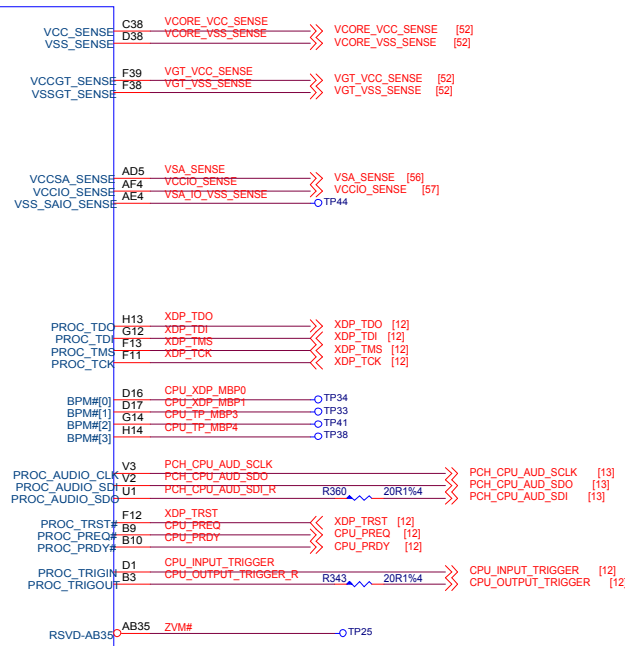
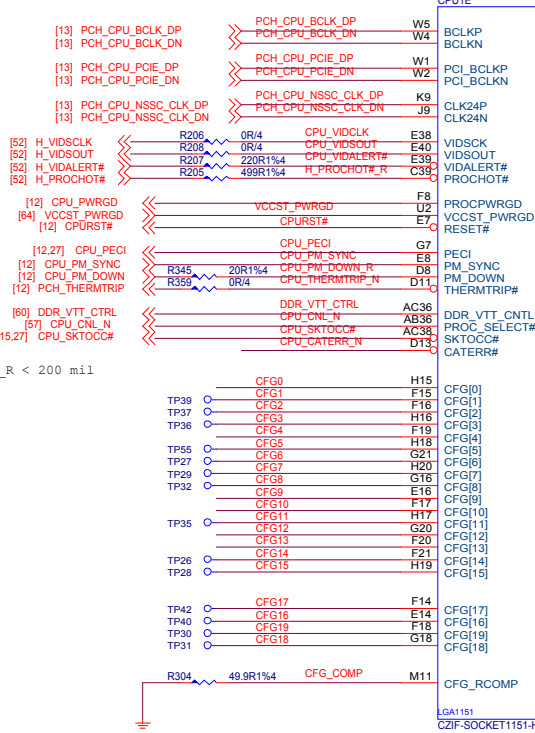
# MS-7B17 Block Diagram

SMBUS ADDRESS:  
VCORE\_PWM:0X8A  
MCU:0X52  
3933:0X20;0X26  
DIMM\_A0:WRITE 0XA0; READ 0XA1  
DIMM\_A1:WRITE 0XA2; READ 0XA3  
DIMM\_B0:WRITE 0XA4; READ 0XA5  
DIMM\_B1:WRITE 0XA6; READ 0XA7





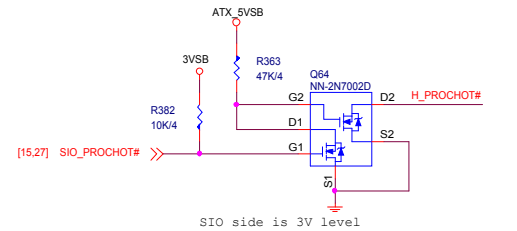
CPU\_PM\_DOWN\_R < 200 mil



## CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	NORM	STALL	EAR
1	NORM	PCHLESS	PCHLESS MODE
2	NORM	REVERSE	PEG LANE REVERSAL
3	ENABLE	DISABLE	DEBUG
4	DISABLE	ENABLE	DP PRESENCE
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG DRIVER TRAINING
8	DISABLE	ENABLE	CFG UNLOCK
9	PRESENT	NO PRESENT	SVID NOT PRESENT
10	ACTIVATE	NO ACTIVATE	SAFE MODE BOOT
11	DC COUPLED	AC COUPLED	DNI AC
12	SPT	NOT SPT	PCH TYPE
13	SVID	FIXED	VCCSA SVID
14	RSVD		
15	RSVD		



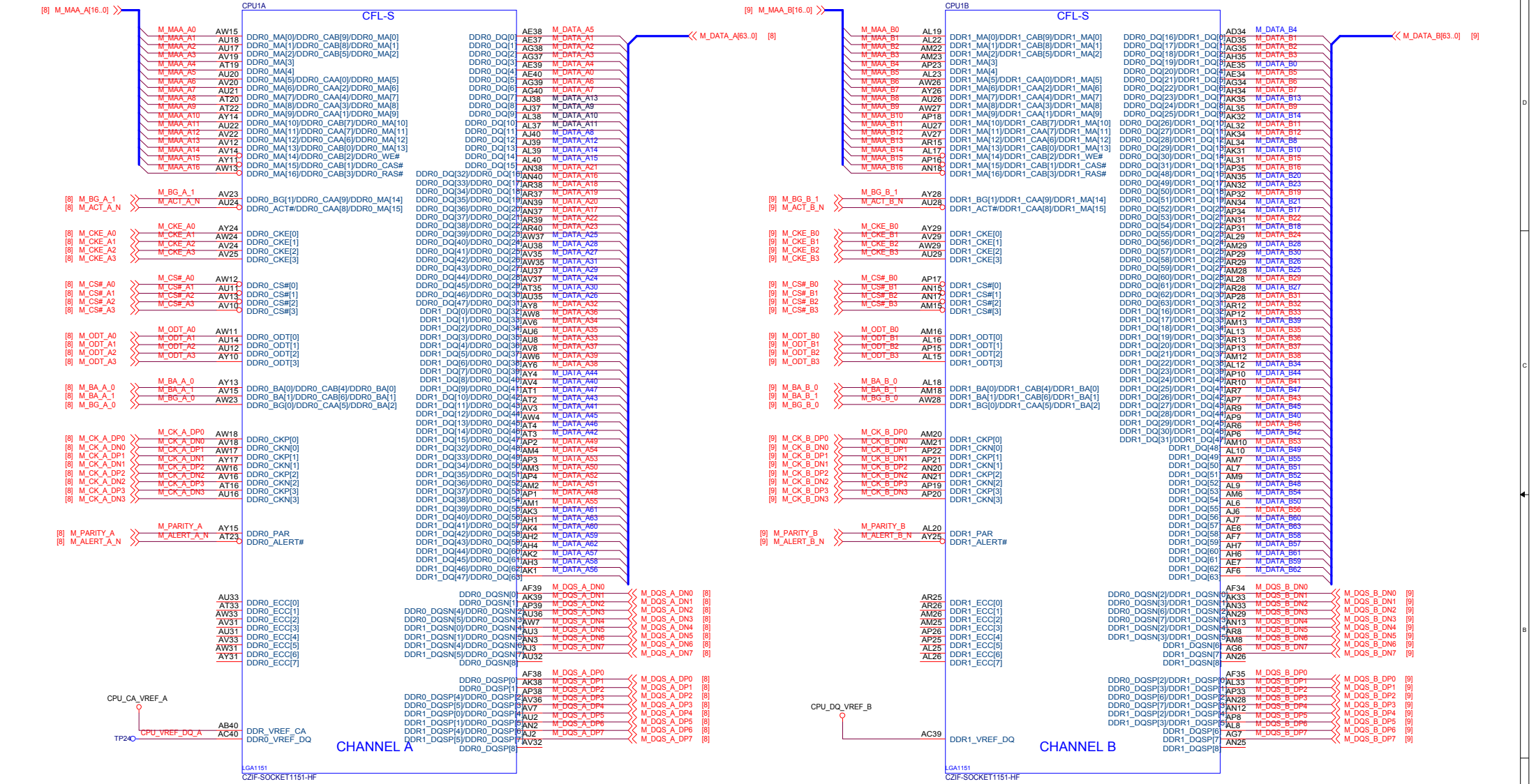
SIO side is 3V level

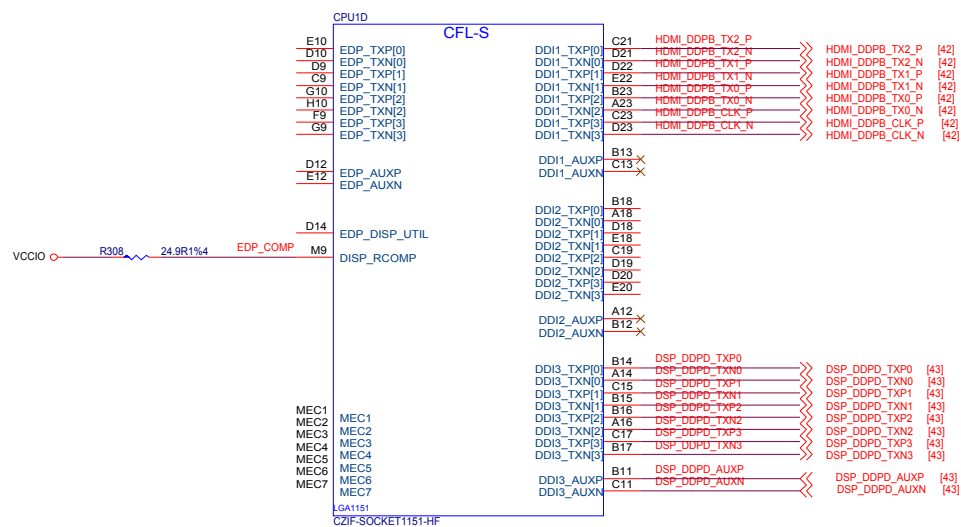
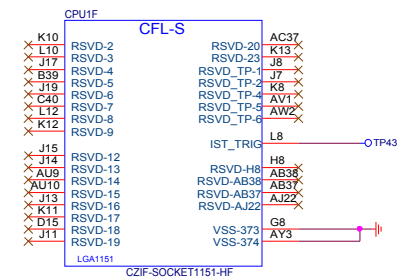
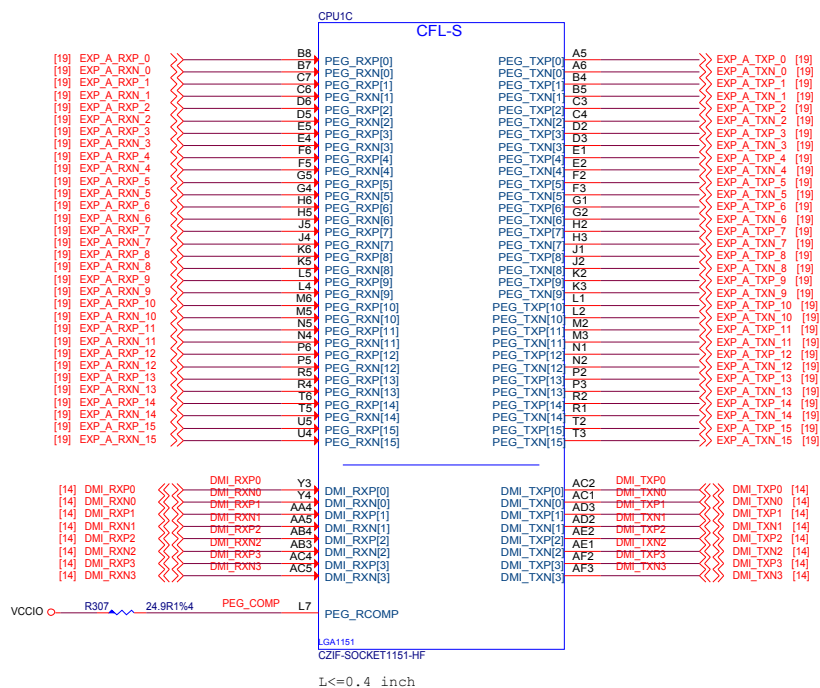
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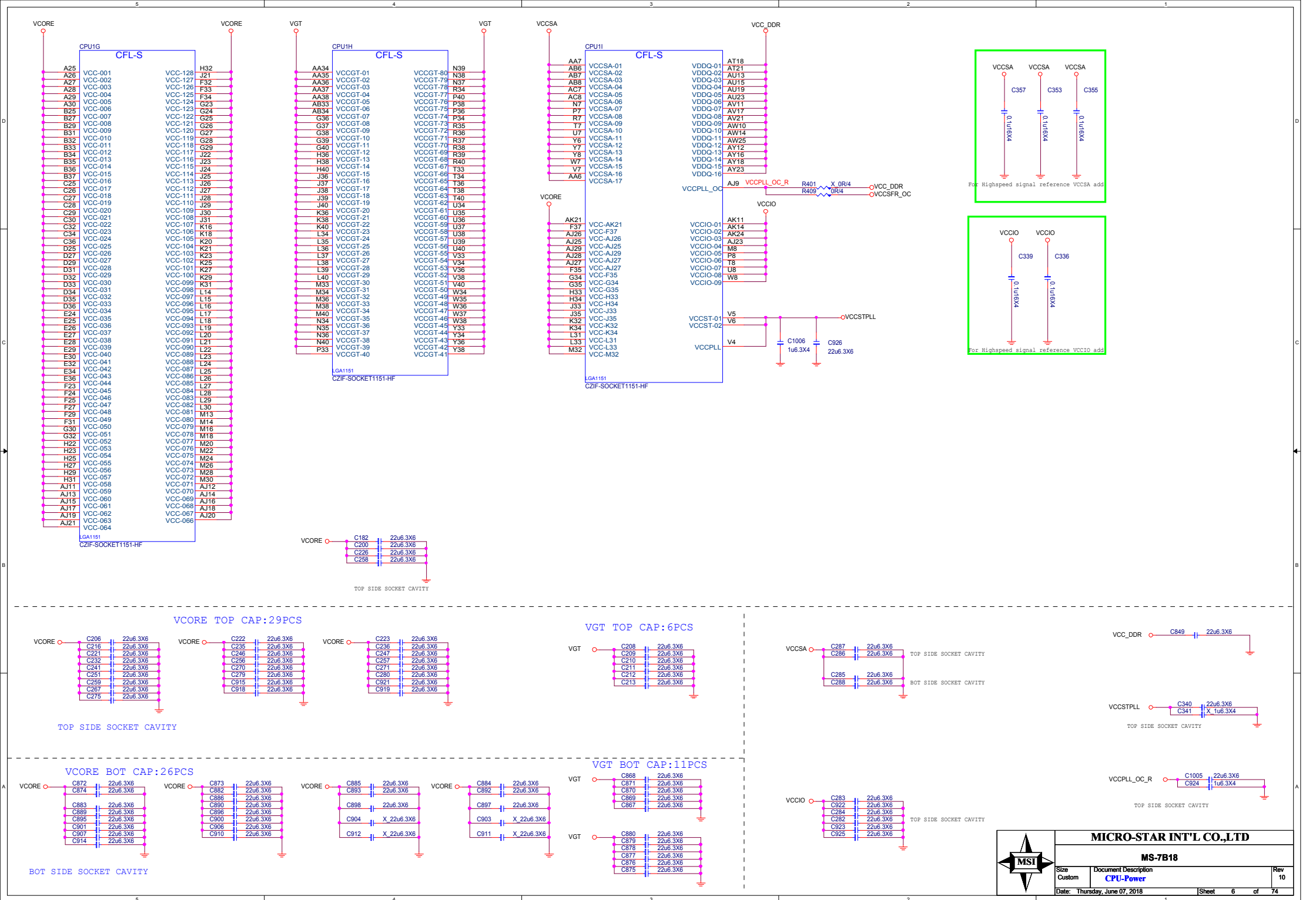
**MS-7B18**

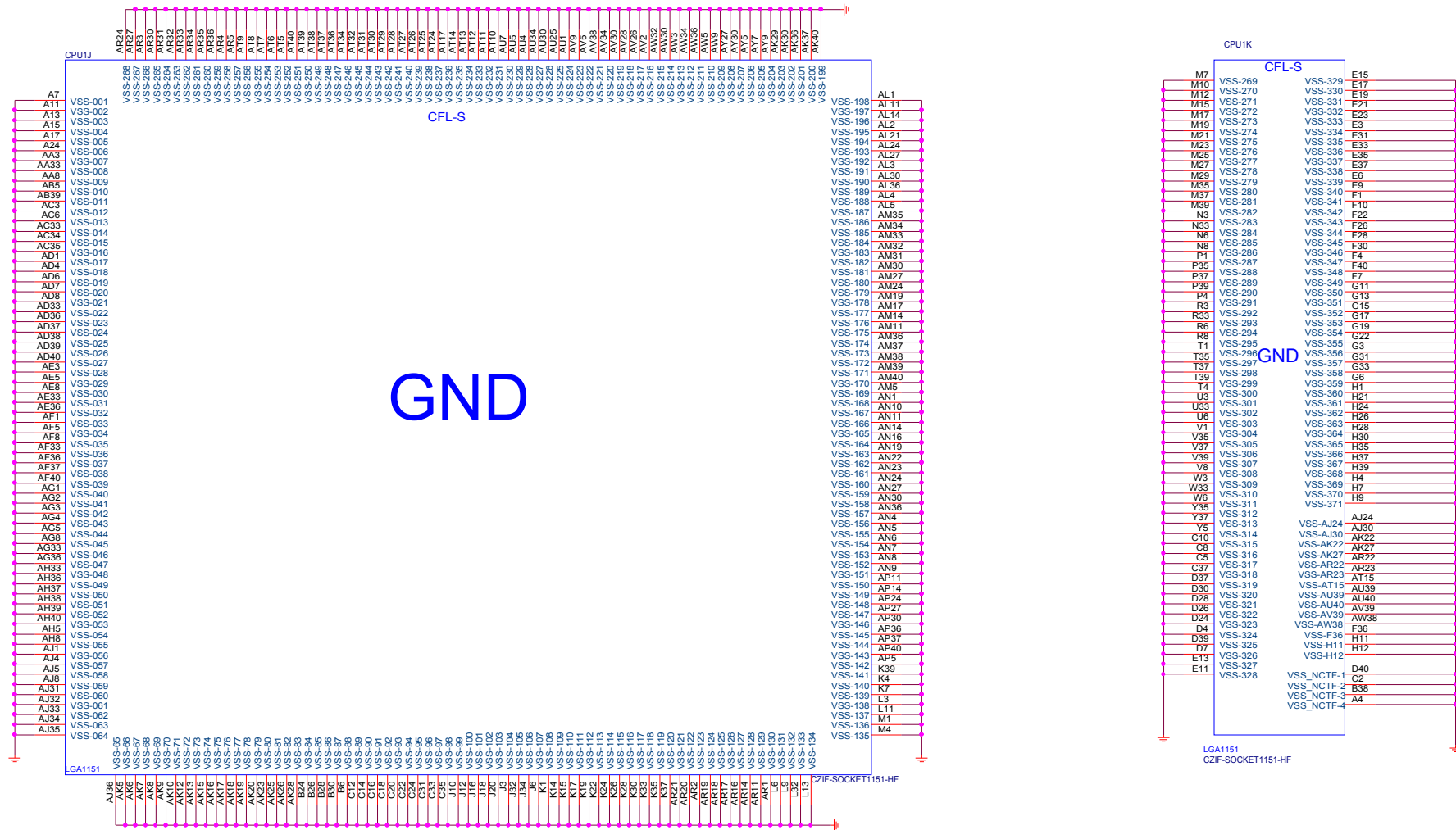
Size Custom Document Description **CPU-Control/MISC/CFG** Rev 10

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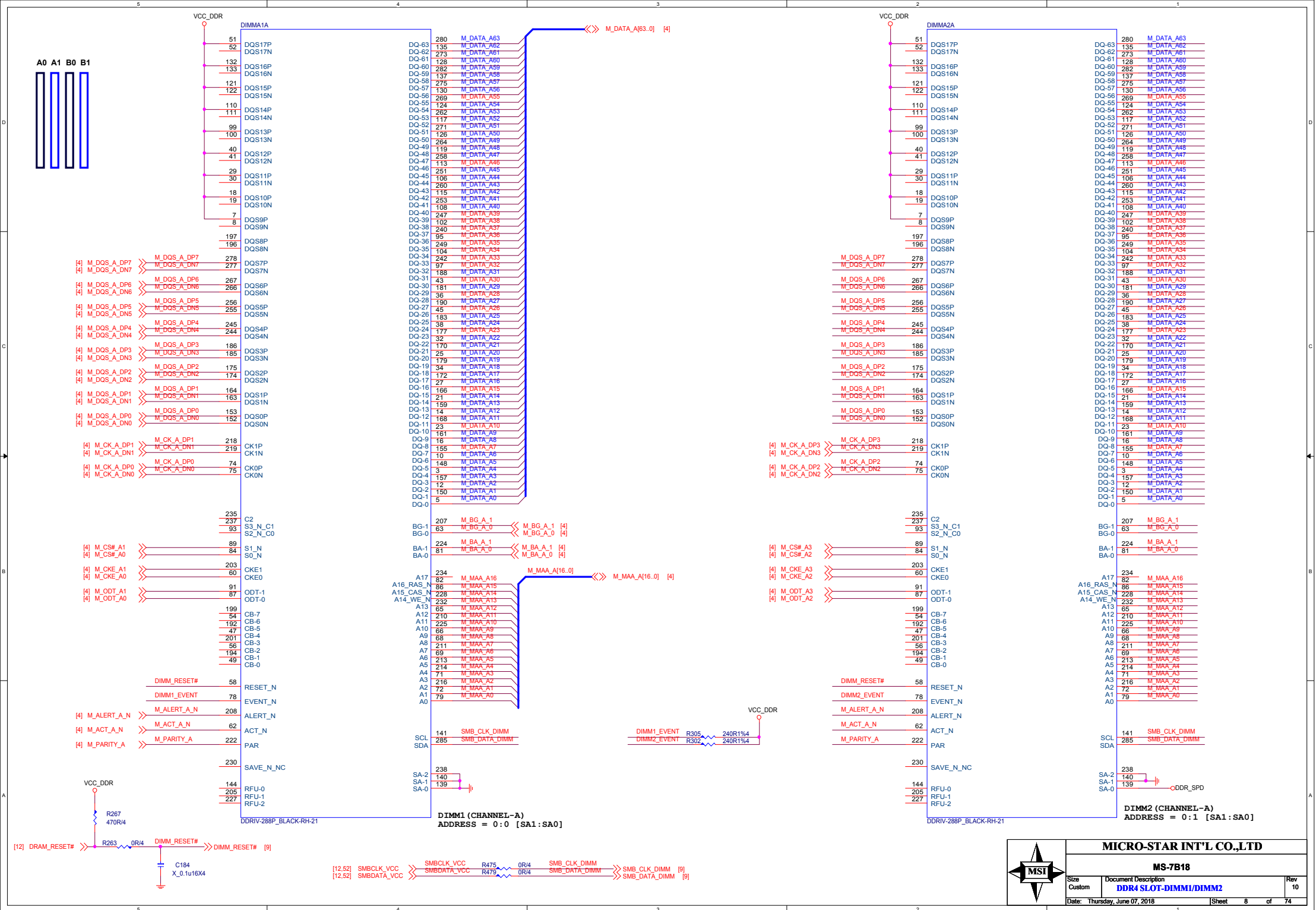






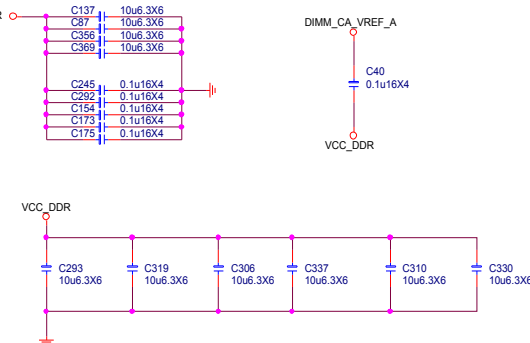
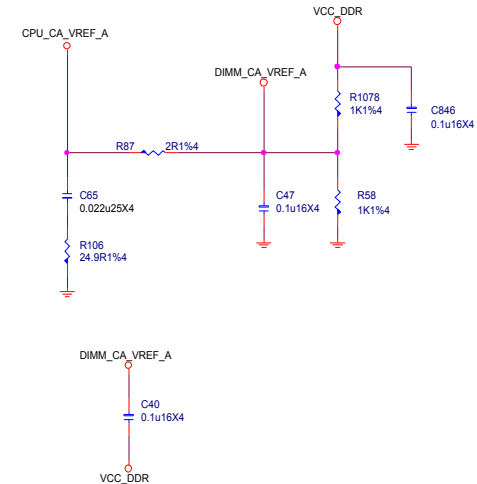
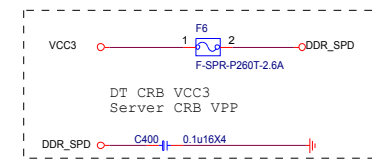
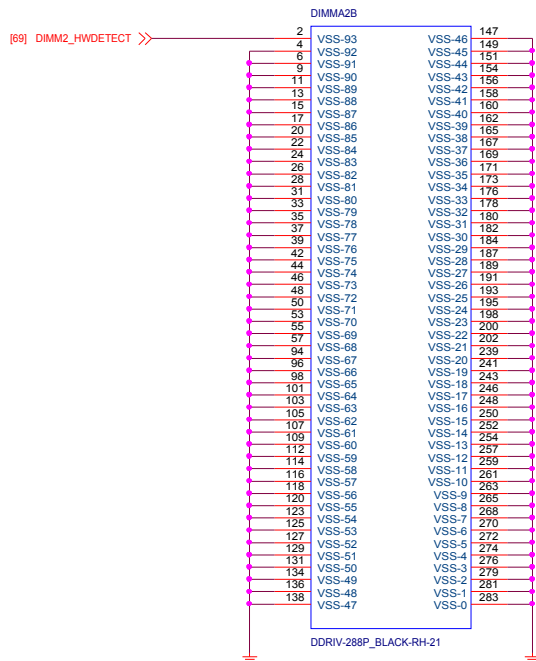
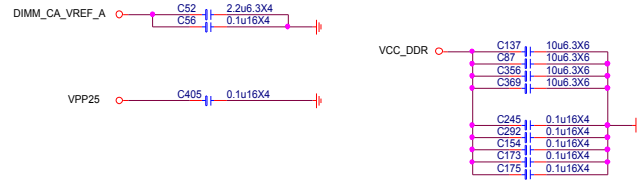
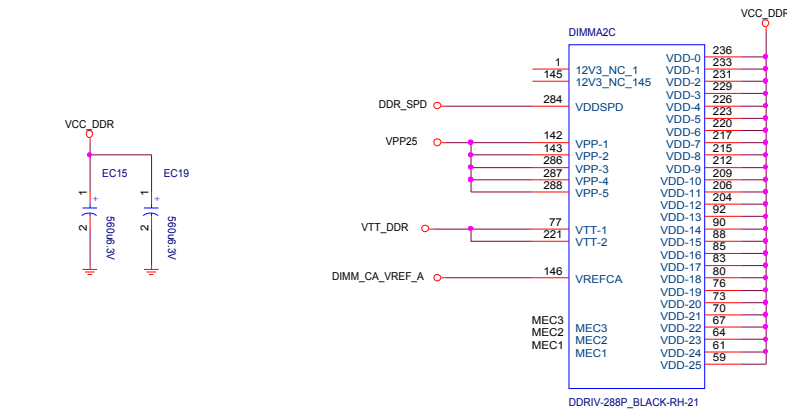
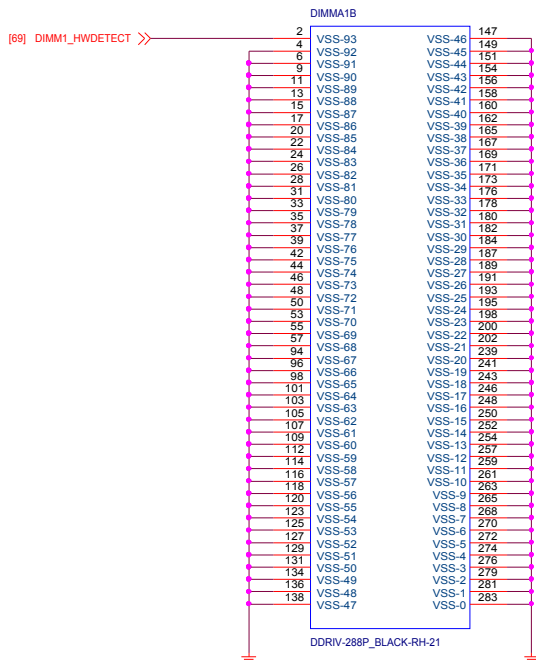
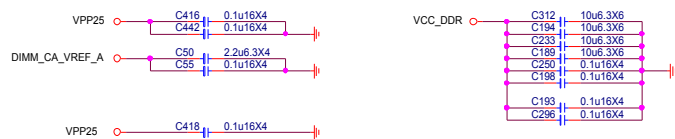
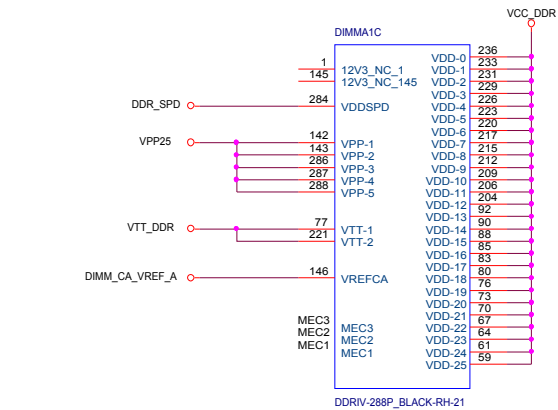


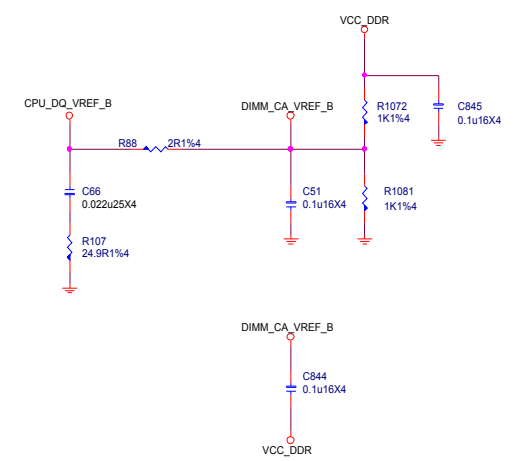
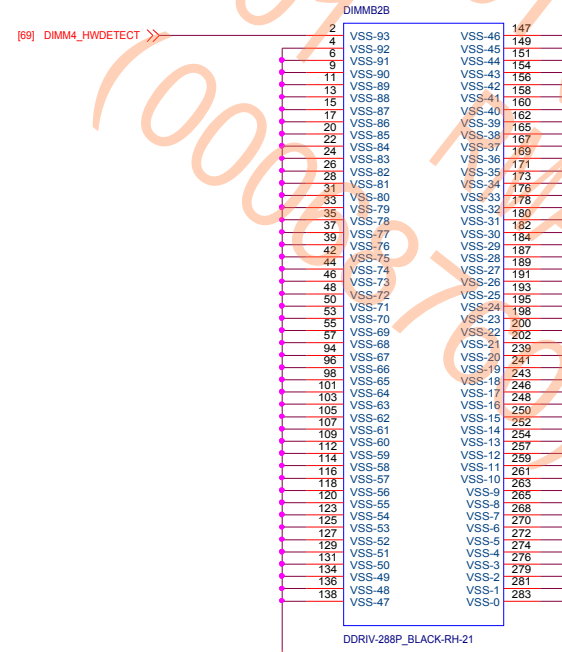
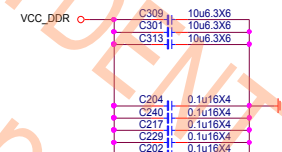
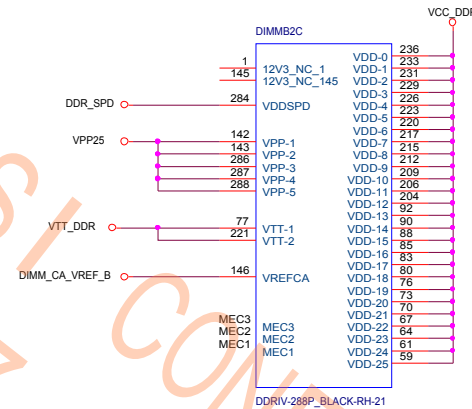
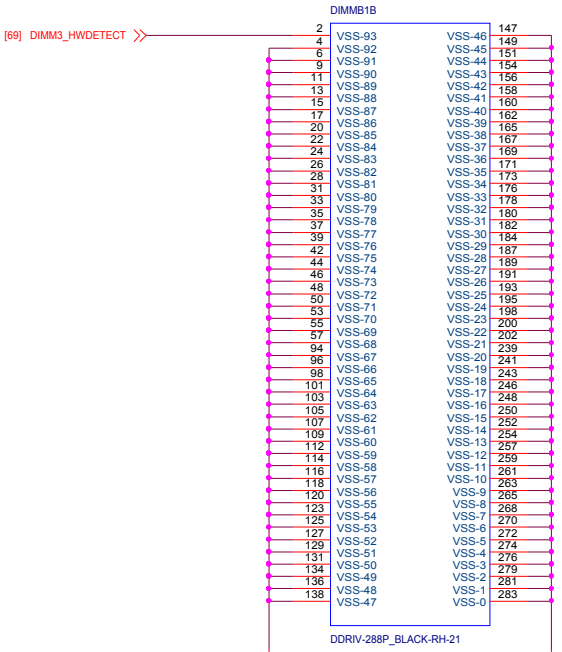
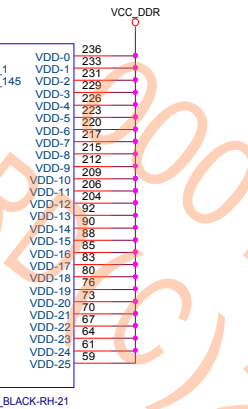
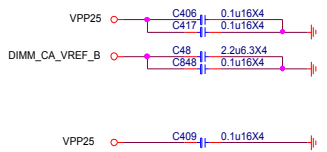
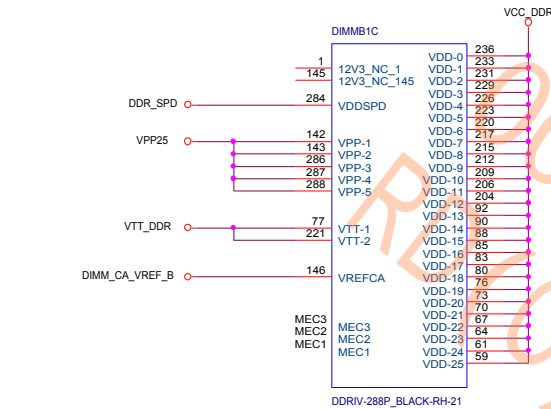




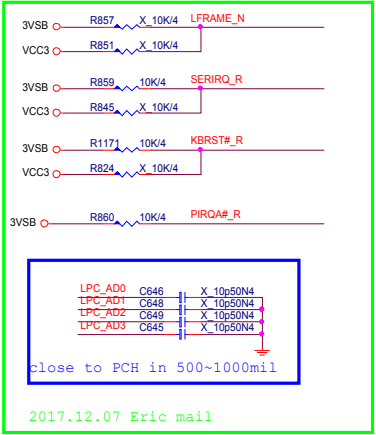








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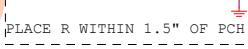
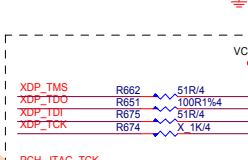
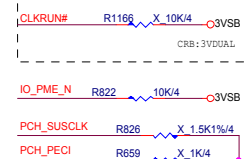
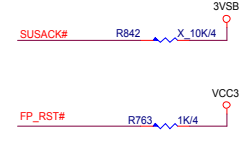
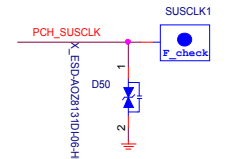
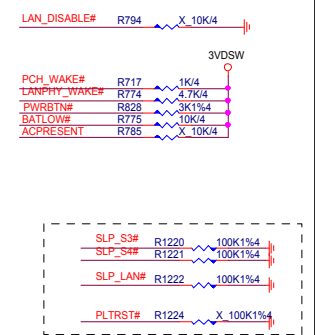
2017.12.07 Eric mail



### Power Management

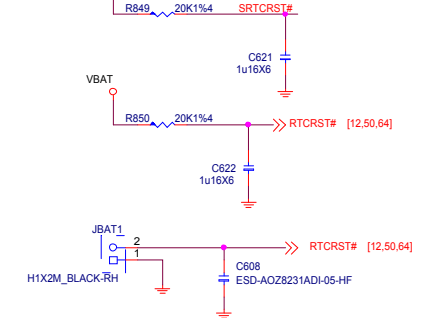
### STRAP

### SPI JTAG

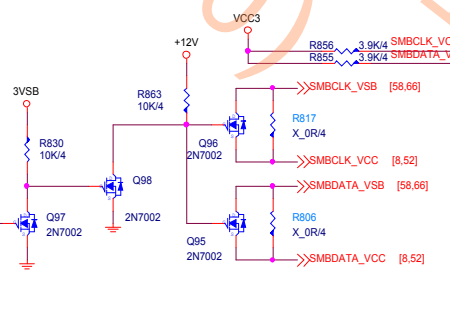
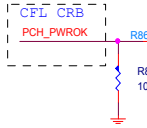
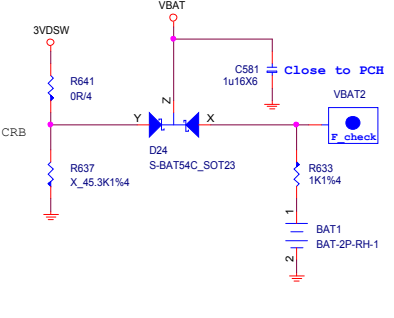


PLACE R WITHIN 1.5" OF PCH

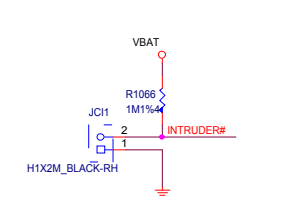
### RTC



### VBAT



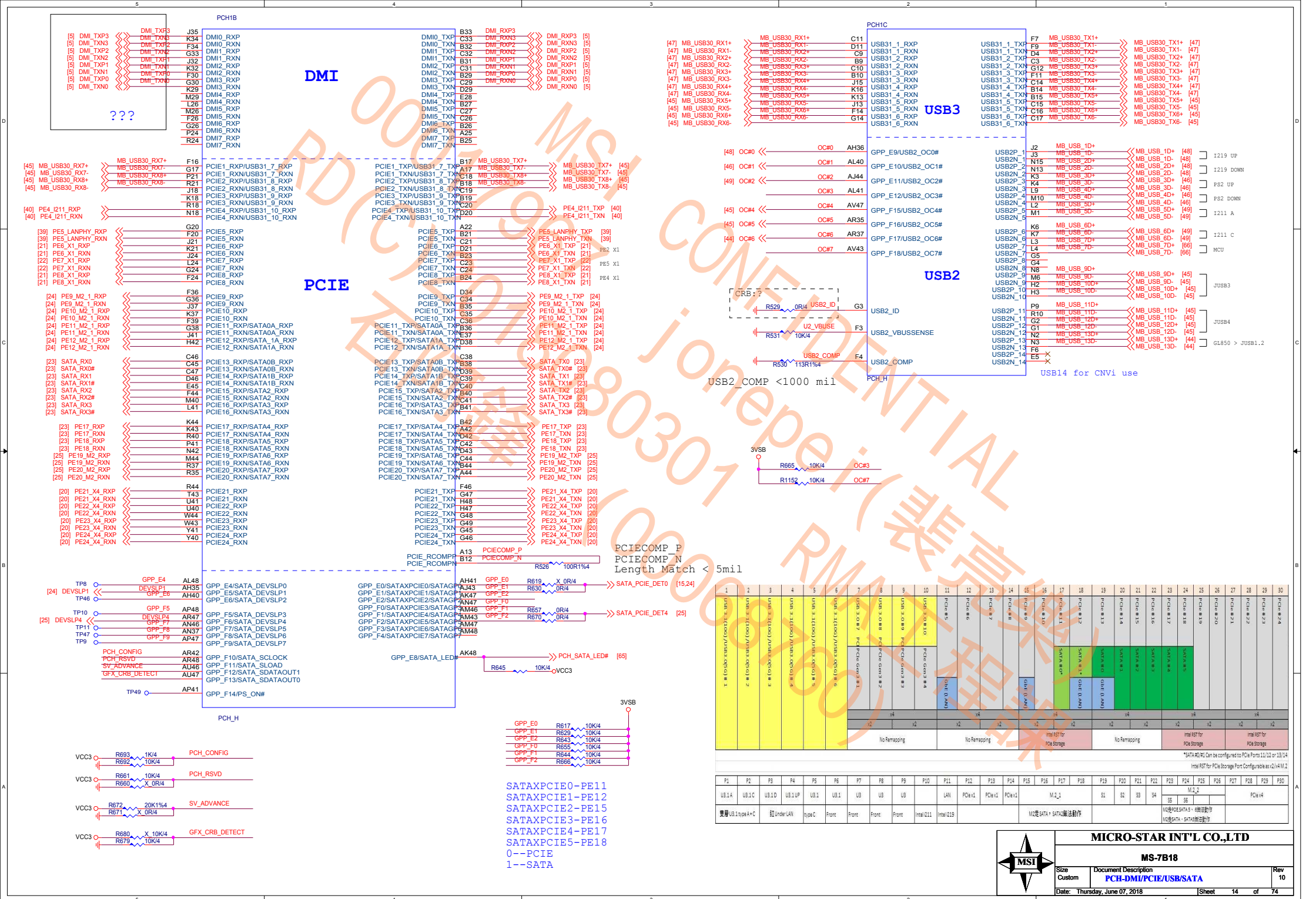
### Chassis Intrusion



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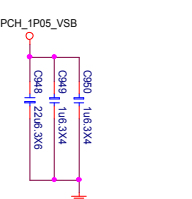
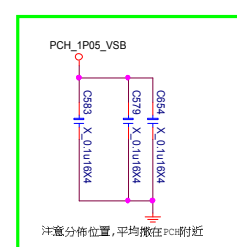
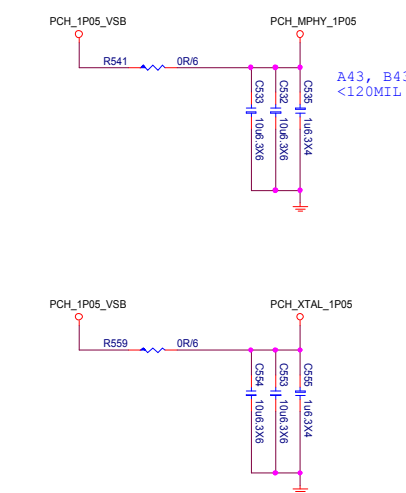




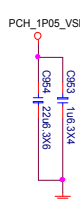




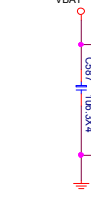
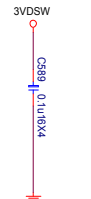
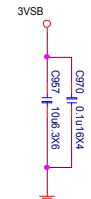
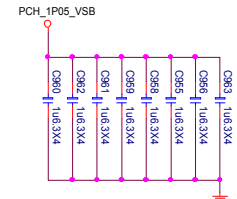




CLOSE TO B1/B2/B3/C1/C2

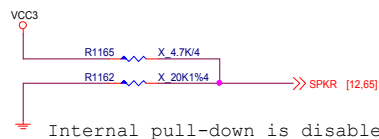


CLOSE TO U26/U29

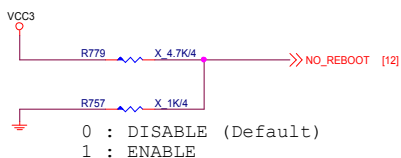


0001-MSI  
RD(C) 018080307  
CONFIDENTIAL  
VSS  
RMA (無記名)

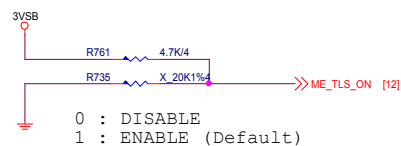
## TOP Swap



## No Reboot

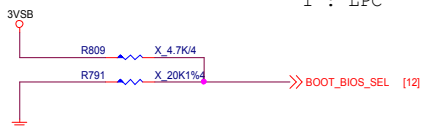


## AMT and SBA with confidentiality

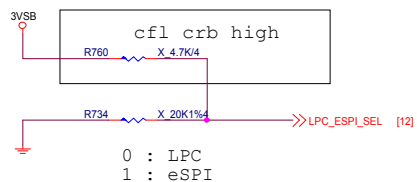


## Boot BIOS

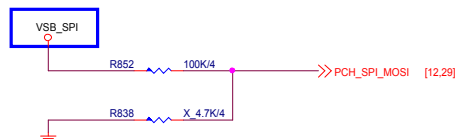
0 : SPI  
1 : LPC



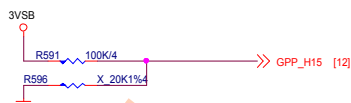
## LPC eSPI Mode



## Reserved



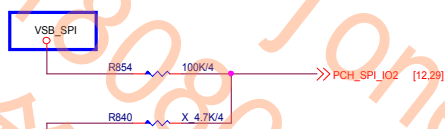
## Reserved



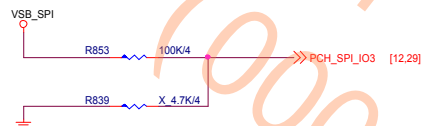
## Reserved



## Reserved

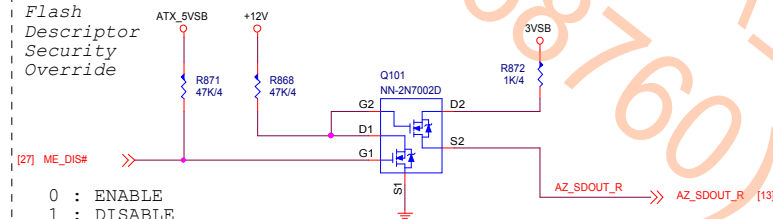


## Reserved

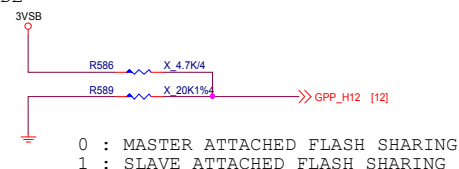


## Flash Descriptor Security Override

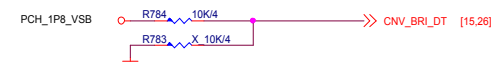
0 : ENABLE  
1 : DISABLE



## eSPI FLASH SHARING MODE

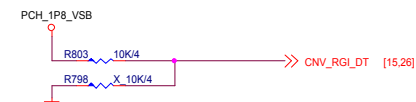


## eSPI FLASH SHARING MODE



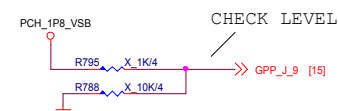
XTAL FREQUENCY SELECTION  
1 = 24MHZ (25MHZ WHEN XTAL FREQ DIVIDER NON ZERO)  
0 = 38.4/19.2MHZ

## Modem Reference Clock Source Select



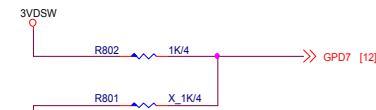
CNL EDS  
0 = Integrated CNVi enable  
1 = Integrated CNVi disable

## 1.8V VCCPSPI



SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE  
0 = VCCPSPI IS CONNECTED TO 3.3V RAIL - DEFAULT  
1 = VCCPSPI IS CONNECTED TO 1.8V RAIL  
PCH HAS INTERNAL 20K PD

## Reserved



XTAL INPUT MODE  
0 = XTAL INPUT IS SINGLE-ENDED  
1 = XTAL INPUT IS DIFFERENTIAL  
PCH HAS INTERNAL 20K PD



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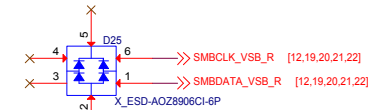
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# PCI Express X16 Slot

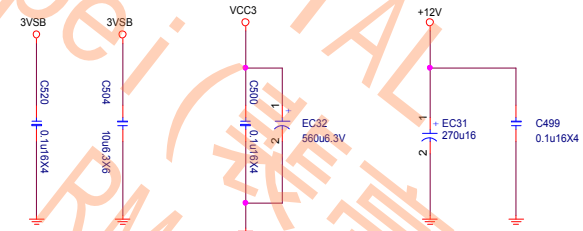
12V - 5.5A  
VCC3 - 3A  
3VSB- 375mA

## SMBUS ESD



By Placement

Main:D0G-05A0529-A68  
AVL:D0G-45B0510-I14



0901 Modify PCI\_E1 PIN X2.X3.X4.X5 Connect to GND

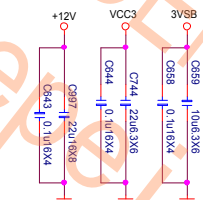


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3VSBV - 375mA

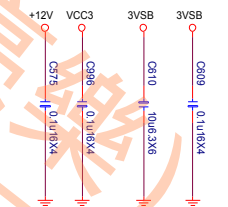
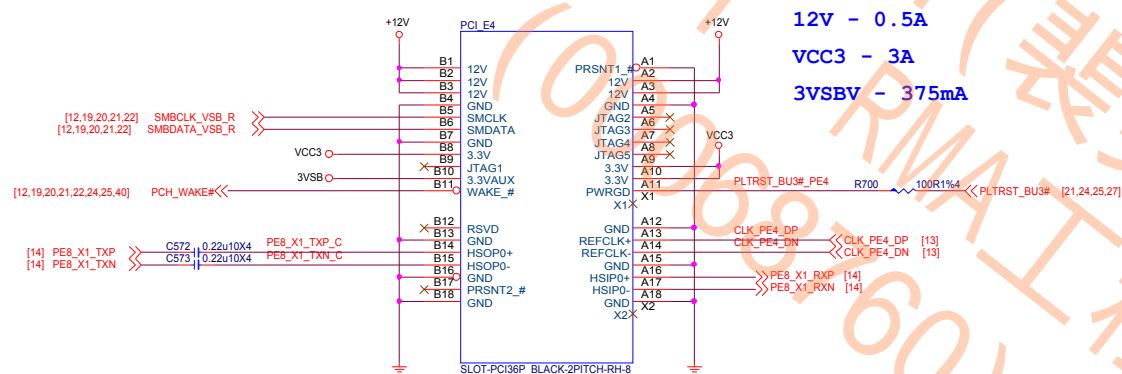
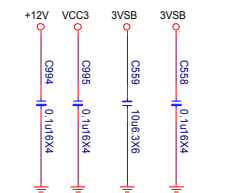
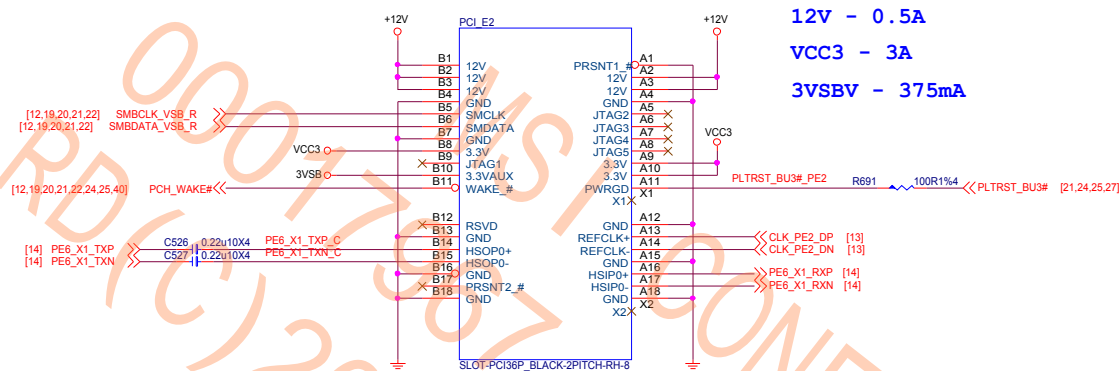


Close to PCI E3 Slot



MS-7B18

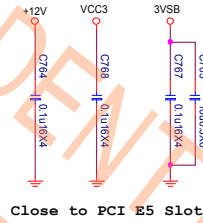
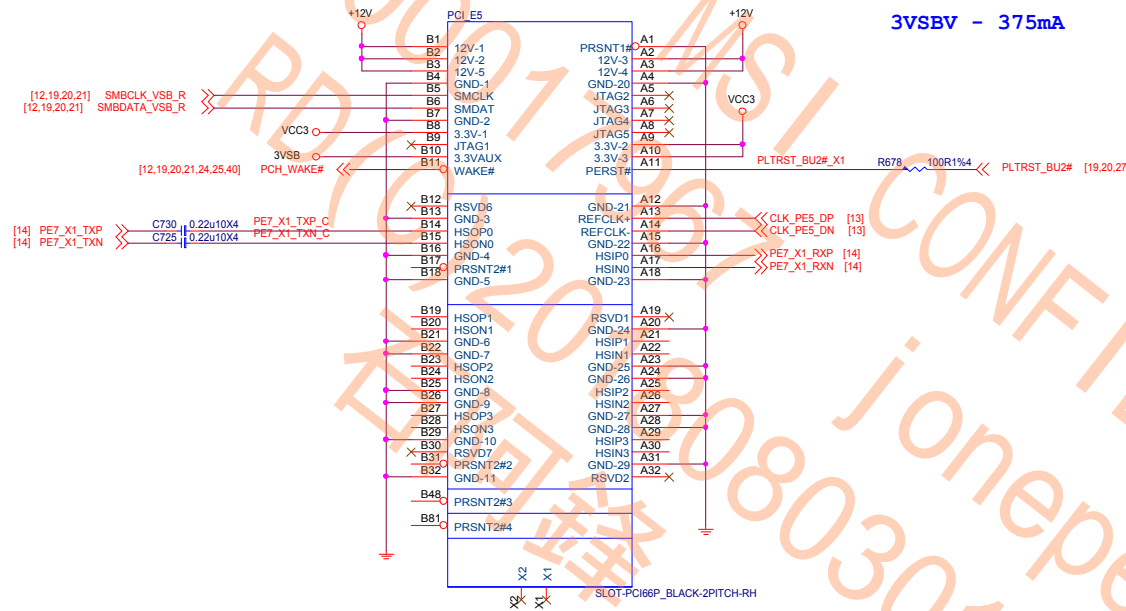
Size Custom	Document Description <b>PCIE SLOT (X4)</b>	Rev 10
Date: Thursday, June 07, 2018		Sheet 20 of 74



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MS-7B18		
Size	Document Description	Rev
Custom	PCIE SLOT (X1)	10
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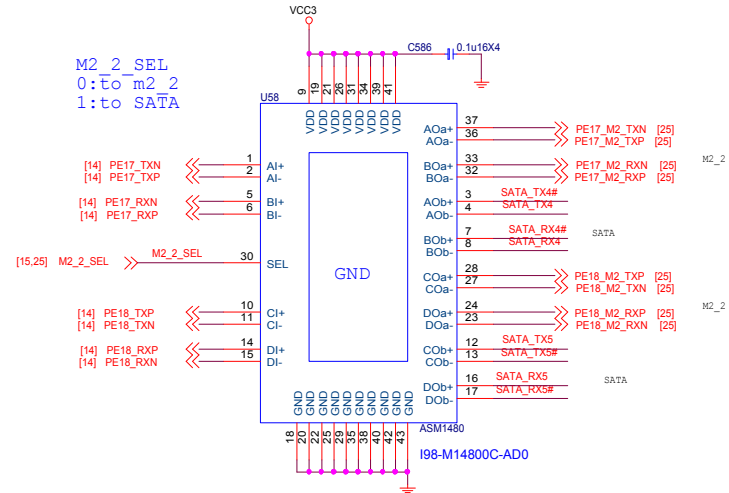
# PCI Express X1 Slot

12V - 2.1A  
VCC3 - 3A  
3VSBV - 375mA

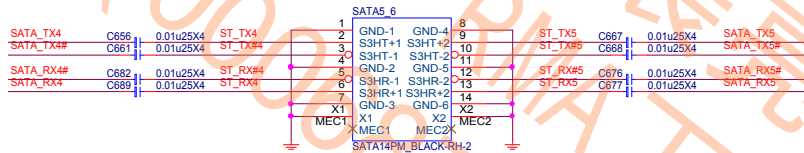




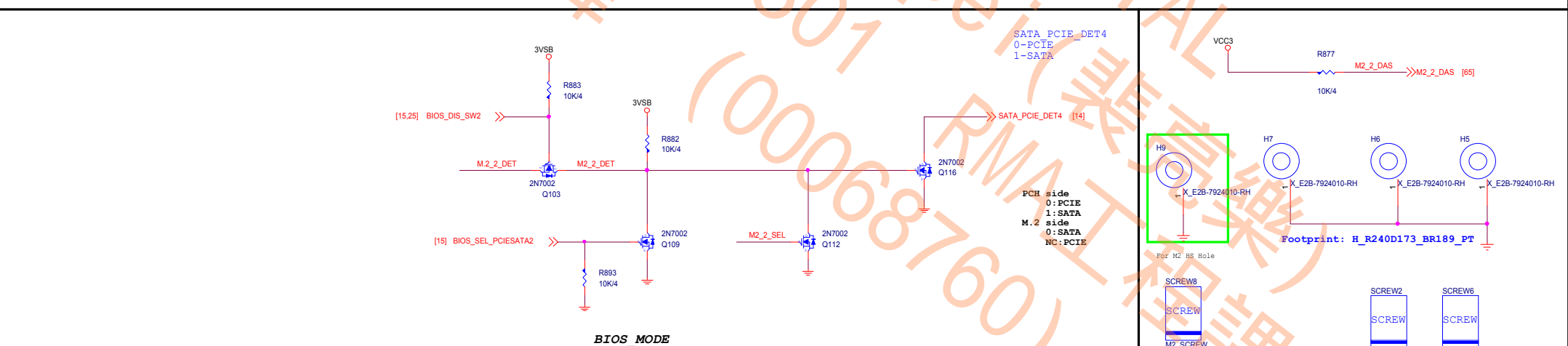
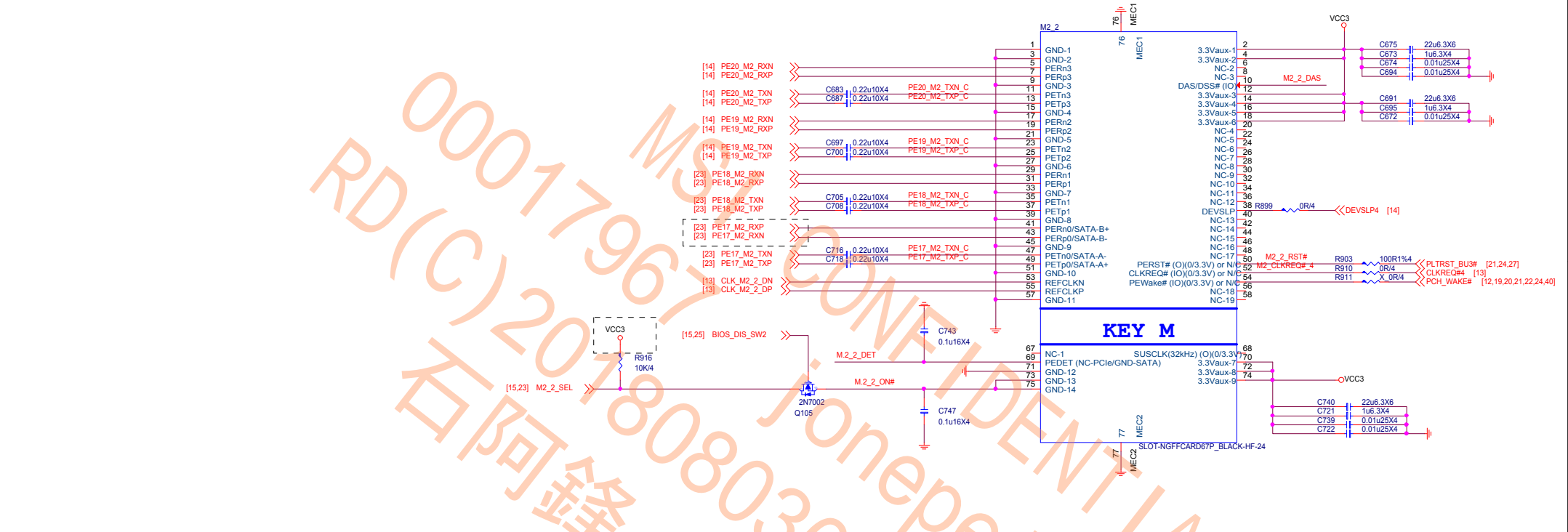
SATA Connector



7B18 2018.04.24 PM Spec modify when M2-SATA Port SATA5,6 no function







HW_MODE				BIOS_MODE			
M2_2_SEL	M2_2_DET	SATA_PCIE_DET4	Mode	BIOS_DIS_SW2	M2_2_SEL	BIOS_SEL_PCIESATA2	Mode
1	1	1	SATA5.6	0	1	0	SATA5
0	0	1	M2-SATA	0	0	1	M2-SATA
0	1	0	M2-PCIE	0	0	0	M2-PCIE

GPP_G7				GPP_G6				GPP_G5			
BIOS_DIS_SW2	M2_2_SEL	BIOS_SEL_PCIESATA2	Mode	BIOS_DIS_SW2	M2_2_SEL	BIOS_SEL_PCIESATA2	Mode	BIOS_DIS_SW2	M2_2_SEL	BIOS_SEL_PCIESATA2	Mode
0	1	0	SATA5	0	0	1	M2-SATA	0	0	0	M2-PCIE
0	0	0	M2-PCIE	0	0	0	M2-PCIE	0	0	0	M2-PCIE

MSI

M2\_SCREW

M2\_SCREW

M2\_SCREW

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MS-7B18

Size Custom

Document Description M2-SLOT2

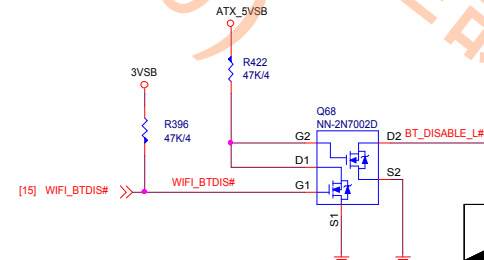
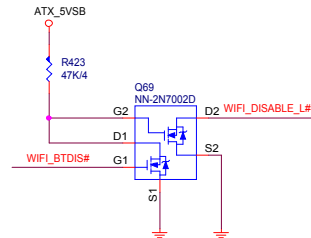
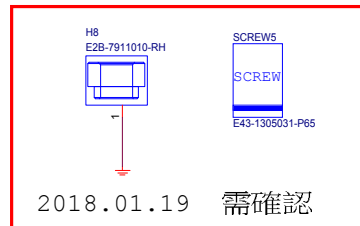
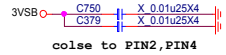
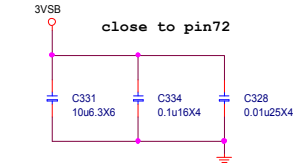
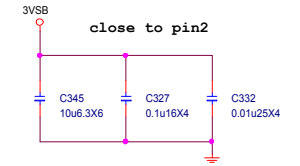
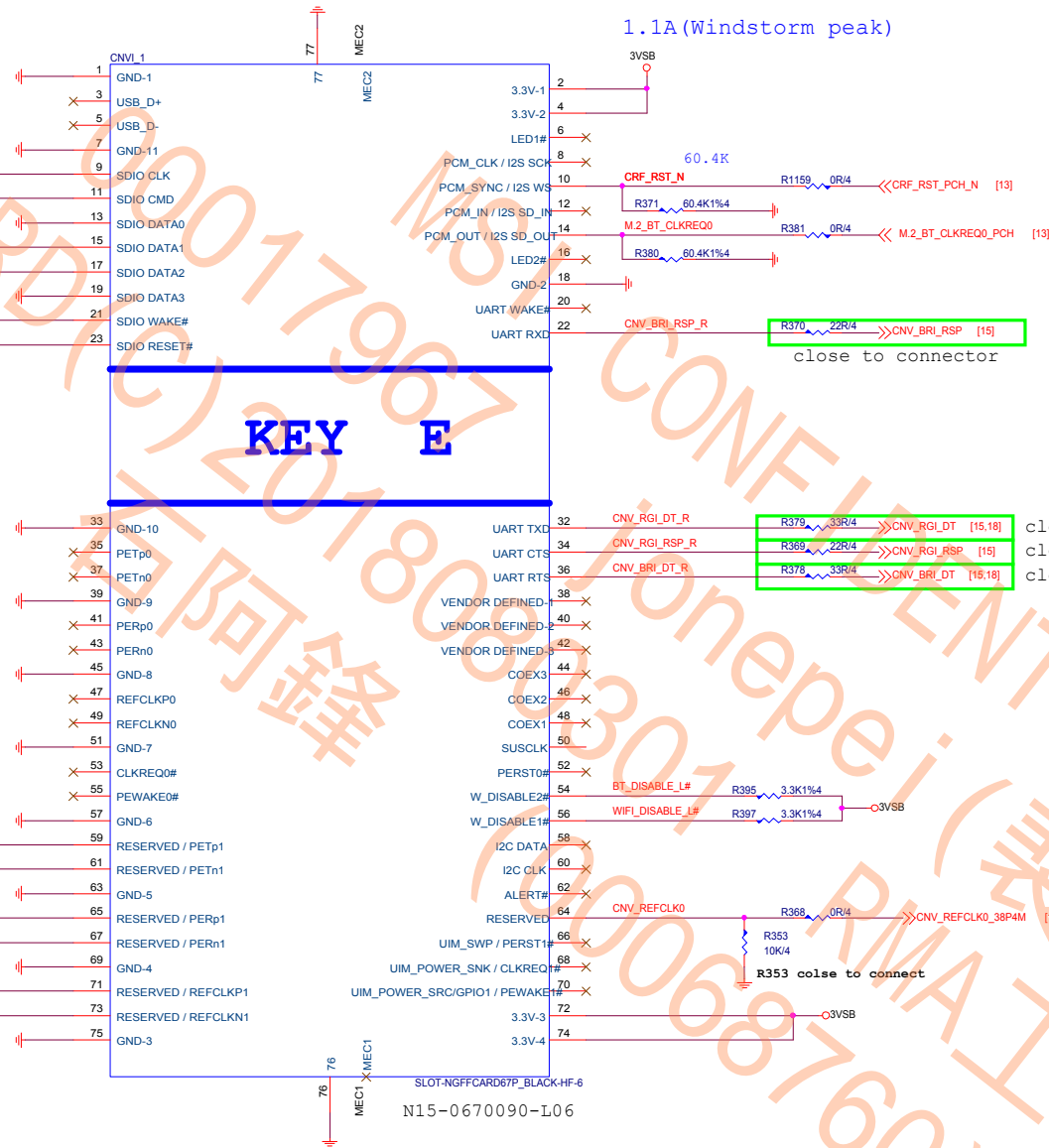
Date: Thursday, June 07, 2018

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[15] CNV\_WR\_1\_DN << R367 0R/4 CNV\_WR\_R\_1\_DN  
[15] CNV\_WR\_1\_DP << R366 0R/4 CNV\_WR\_R\_1\_DP  
[15] CNV\_WR\_0\_DN << R352 0R/4 CNV\_WR\_R\_0\_DN  
[15] CNV\_WR\_0\_DP << R351 0R/4 CNV\_WR\_R\_0\_DP  
[15] CNV\_WR\_CLK\_DN << R365 0R/4 CNV\_WR\_R\_CLK\_DN  
[15] CNV\_WR\_CLK\_DP << R364 0R/4 CNV\_WR\_R\_CLK\_DP

[15] CNV\_WT\_1\_DN << R350 0R/4 CNV\_WT\_R\_1\_DN  
[15] CNV\_WT\_1\_DP << R349 0R/4 CNV\_WT\_R\_1\_DP  
[15] CNV\_WT\_0\_DN << R373 0R/4 CNV\_WT\_R\_0\_DN  
[15] CNV\_WT\_0\_DP << R372 0R/4 CNV\_WT\_R\_0\_DP  
[15] CNV\_WT\_CLK\_DN << R348 0R/4 CNV\_WT\_R\_CLK\_DN  
[15] CNV\_WT\_CLK\_DP << R347 0R/4 CNV\_WT\_R\_CLK\_DP



POWER ON STRAPPING PIN FOR NCT6797					
PIN	NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	DDR4_EN	DDR4_EN	Disable	Enable	
27	ESPI_EN	A20GATE	LPC	ESPI	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	FANOUT_DEF_EN	DTRA#	default 50%	default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMPDWR_EN	AMPDWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

#### Note:

If PIN34 strapping low, BIOS must programming LPT or GPIO

#### 3V Analog Power

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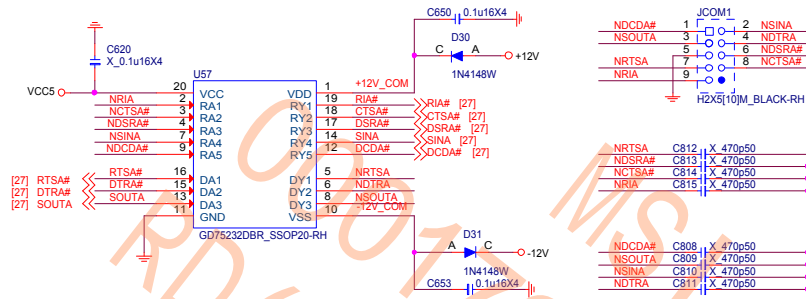
Size	Document Description	Rev
Custom	SIO-NCT6793D-1	
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## SERIAL PORT 1

SIO\_VCC3

R765 X 2.7K SINA  
R707 X 2.7K CTSA#  
R746 X 2.7K RIA#  
R767 X 2.7K DCSA#  
R715 X 2.7K DSRA#

NO USE UART PORT1

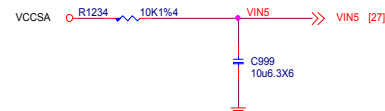
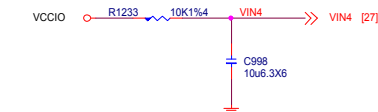
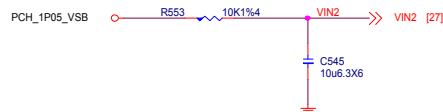
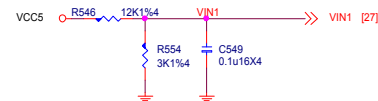
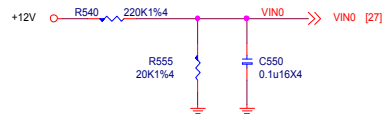
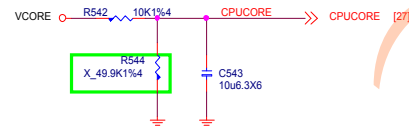
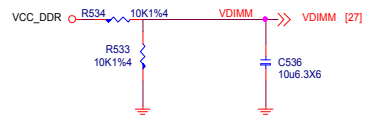


RSMRST# USE solution

2017.11.30 robert\_mail remove

## HW Monitor - Voltage

SIO HM Voltage voer 2V will not detect



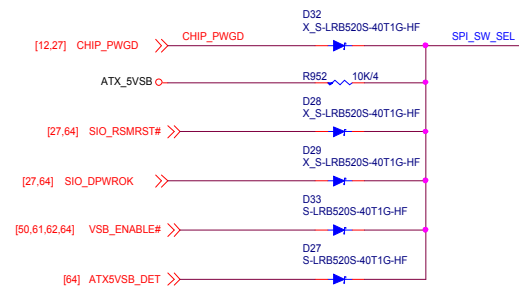
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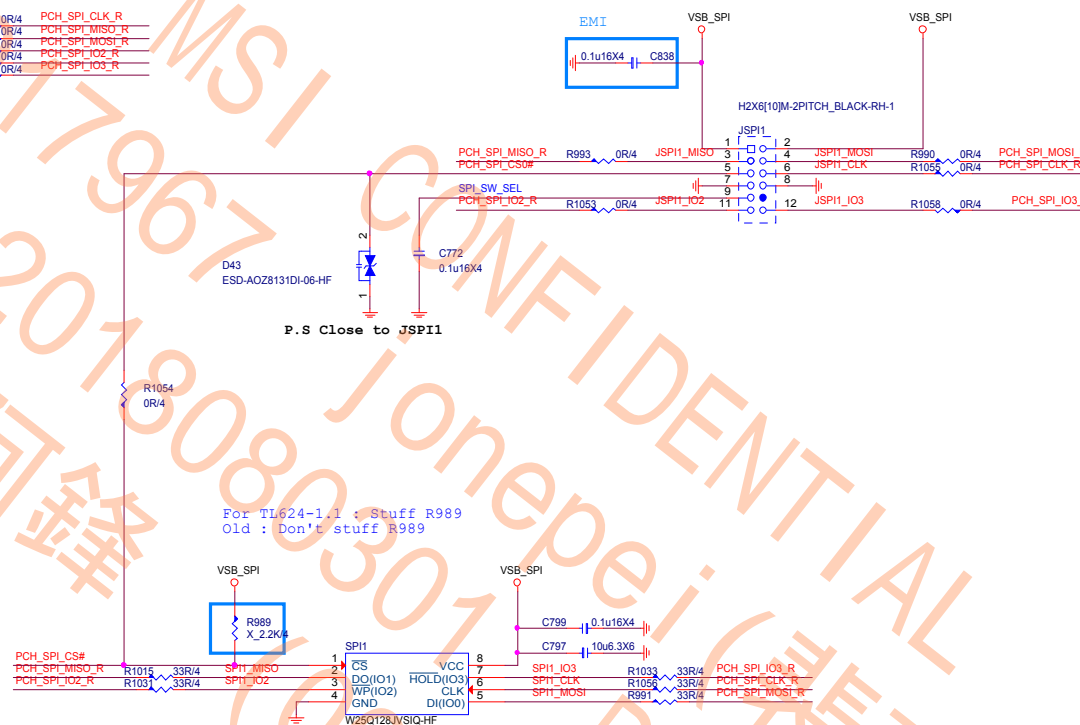
Size	Document Description	Rev
Custom	SIO-NCT6793D-2	10
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Module Stuff CHIP\_PWGD,  
But PCH PWROK may ramp up before CHIP\_PWGD.

For T1624 1.1



```
SKYLAKE : Stuff D10/D17/R353
B85/H87 : Stuff D8/D9/R353
Others  : Stuff R272
```



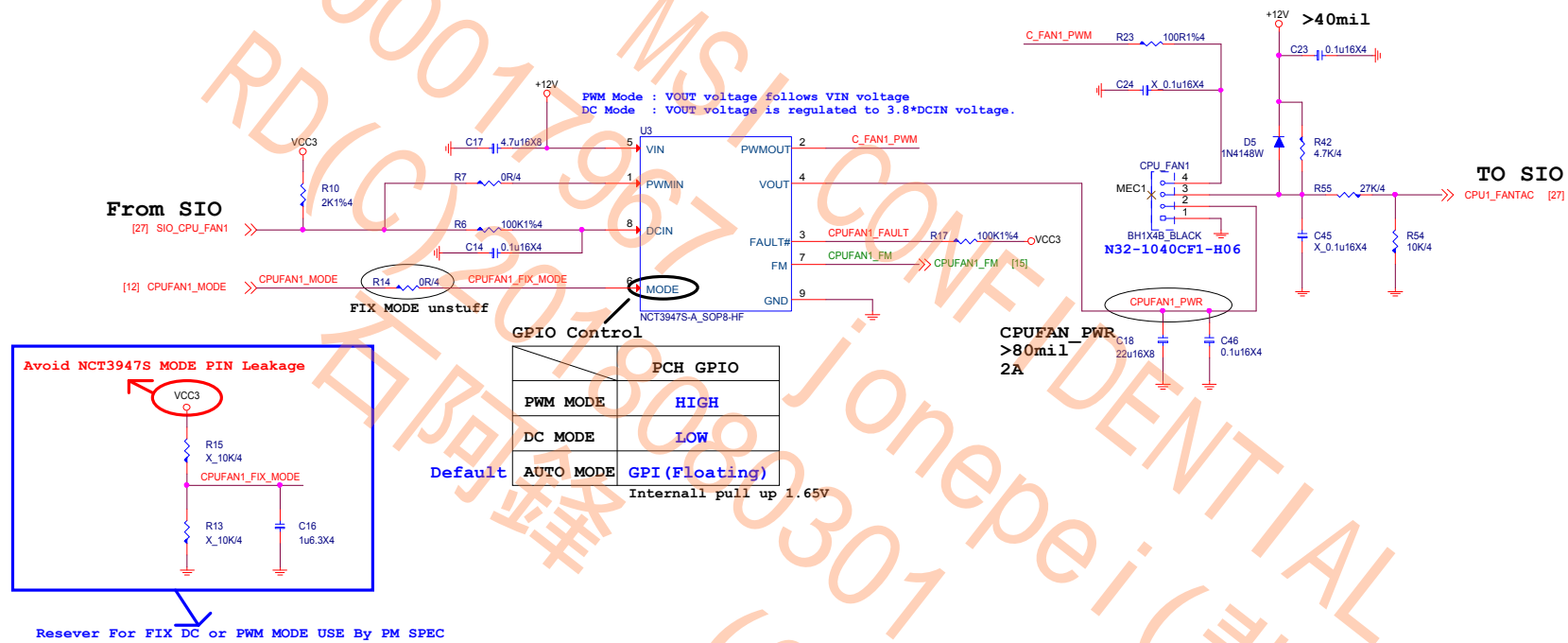
**MS-7B18**

Size Custom	Document Description <b>Dual BIOS</b>	Rev 16
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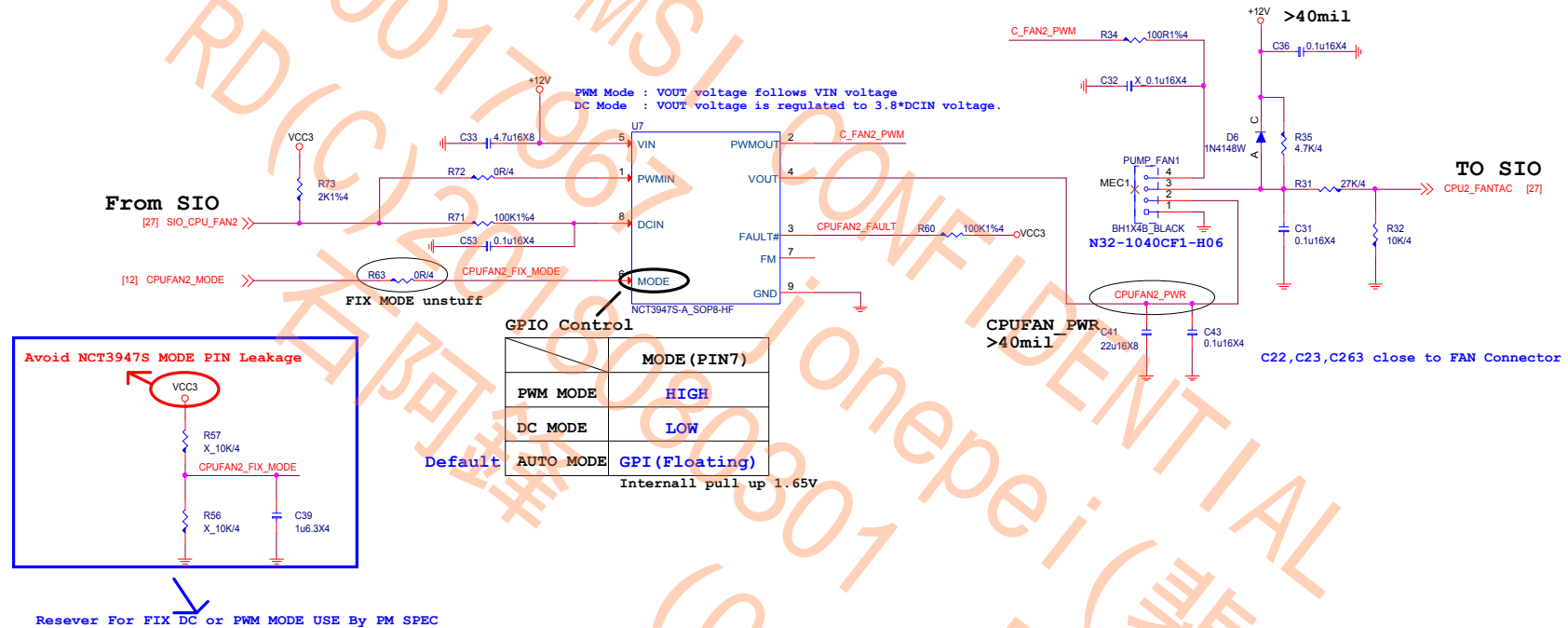


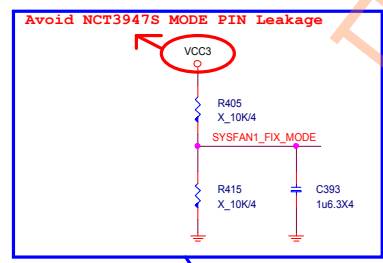
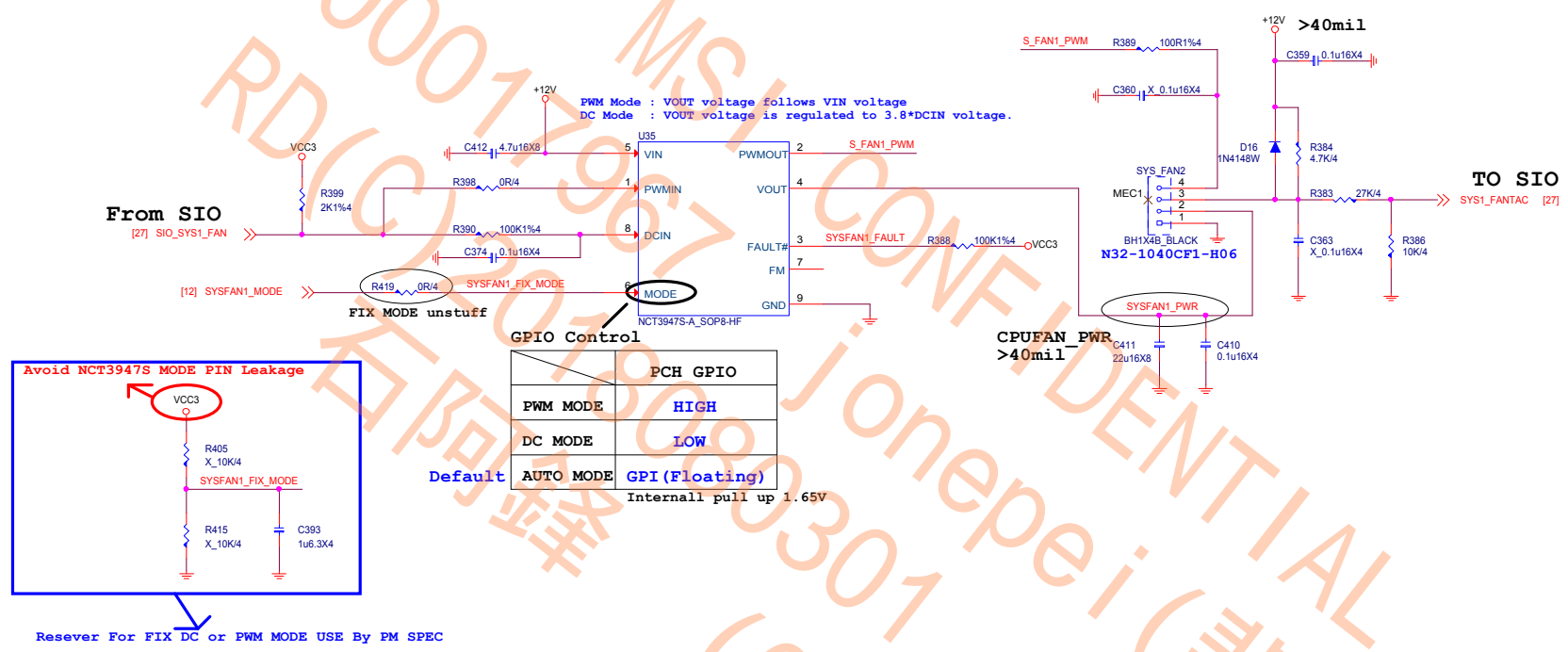
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1.Mode GPIO BIOS can swtich PWM/DC MODE

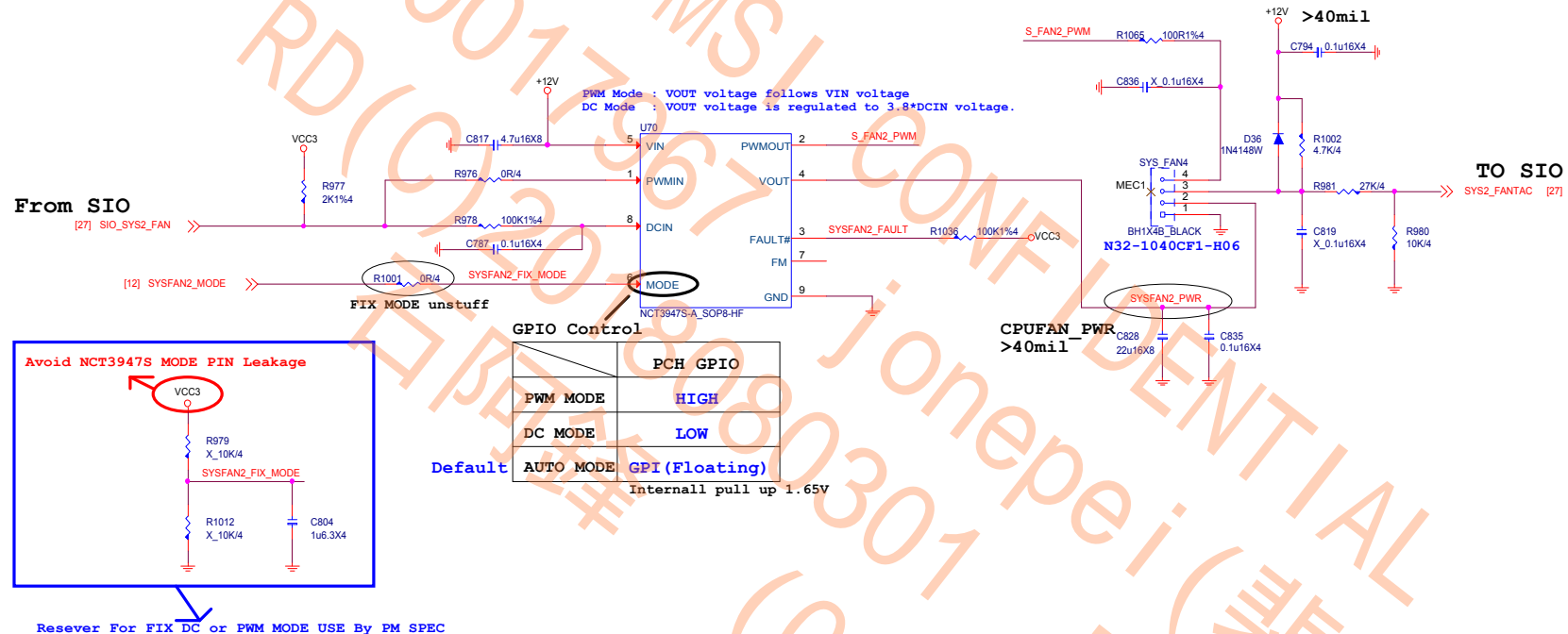


## 1.Mode GPIO BIOS can switch PWM/DC MODE

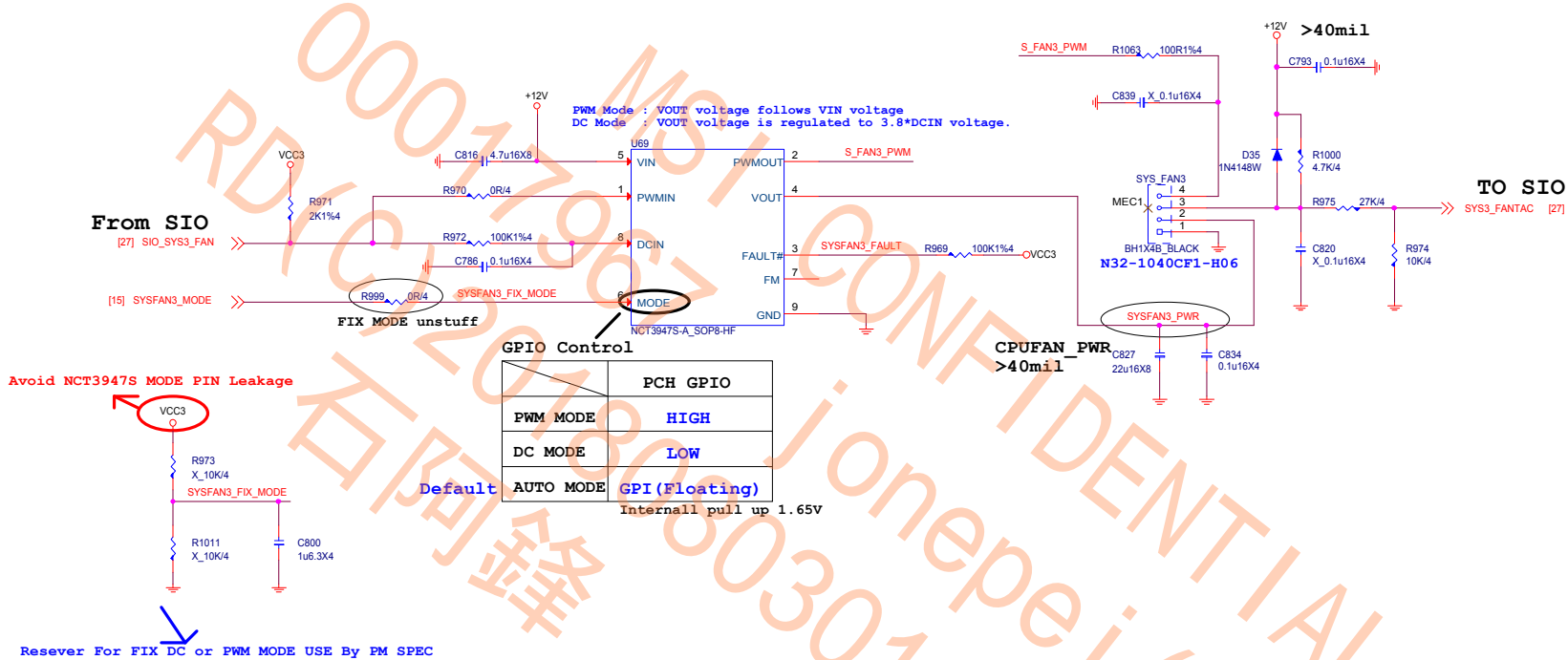




TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE  
 1.Mode GPIO BIOS can switch PWM/DC MODE

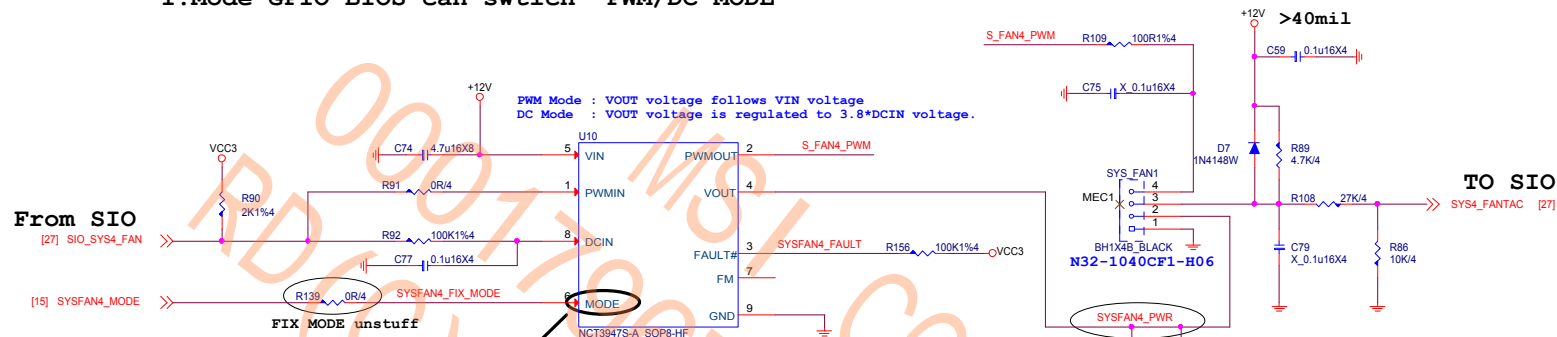


TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE  
1.Mode GPIO BIOS can switch PWM/DC MODE

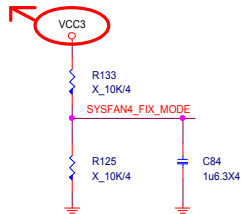


# TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

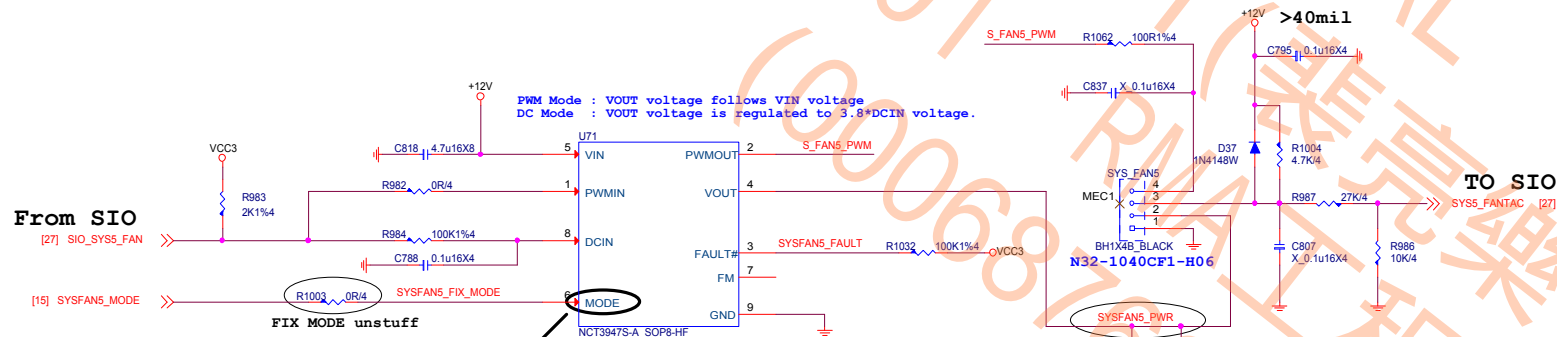
## 1.Mode GPIO BIOS can swtich PWM/DC MODE



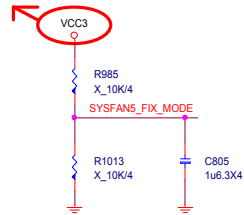
### Avoid NCT3947S MODE PIN Leakage



Resever For FIX DC or PWM MODE USE By PM SPEC



### Avoid NCT3947S MODE PIN Leakage



Resever For FIX DC or PWM MODE USE By PM SPEC

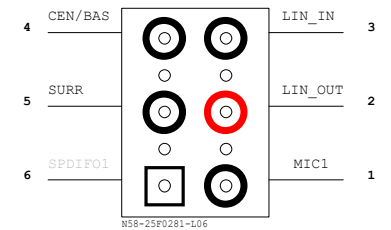
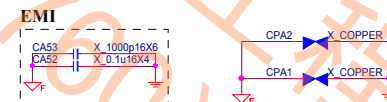
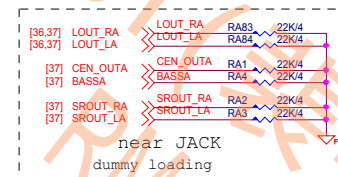
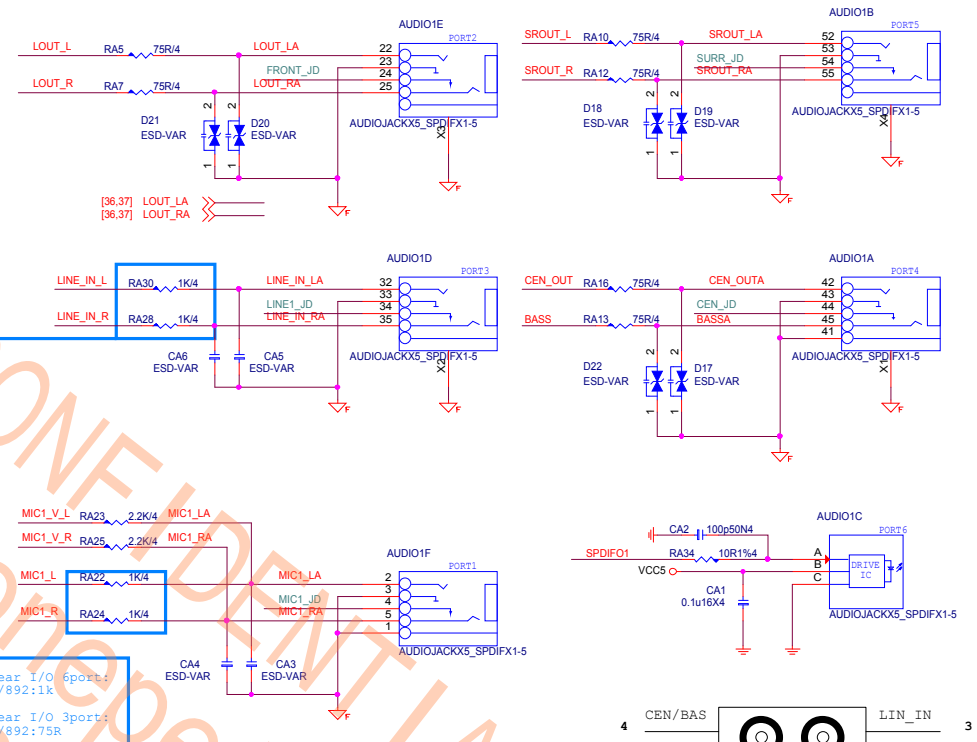
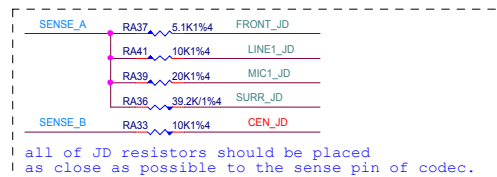
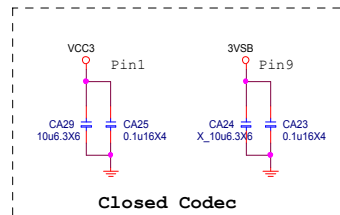
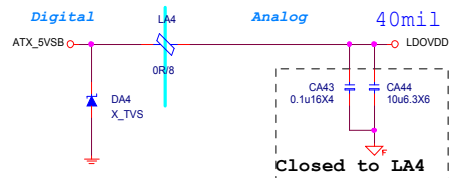
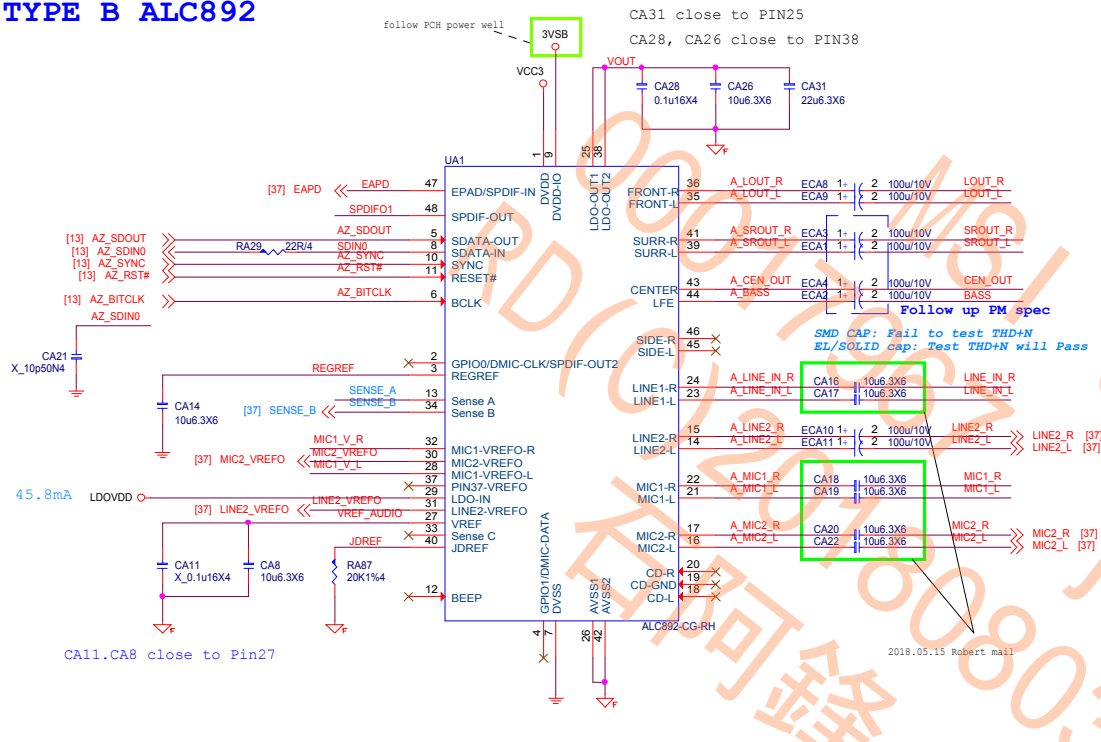


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**TYPE B ALC892**

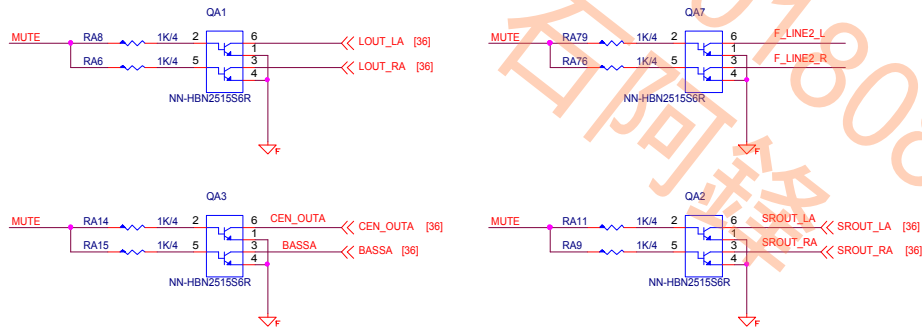
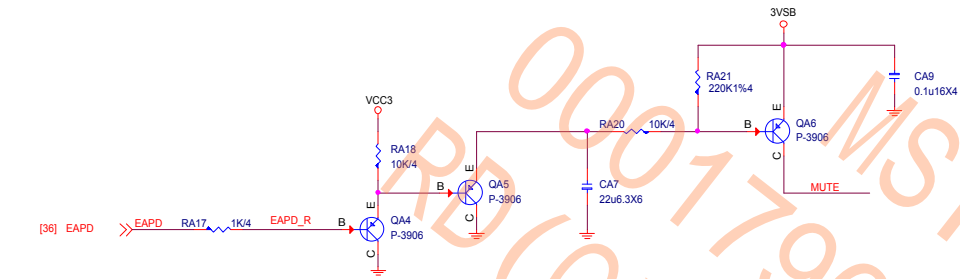




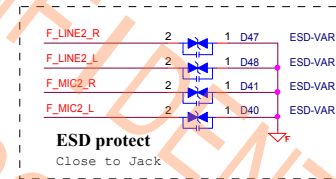
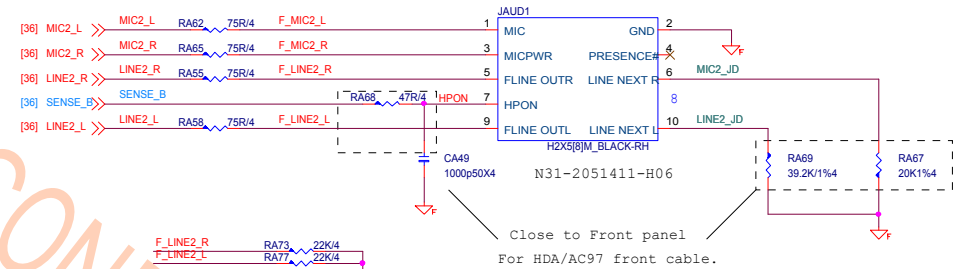
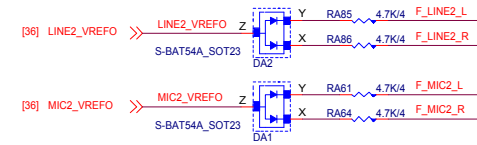
Rear Line OUT De-POP circuit  
(De-pop circuit for Rear Line out & Front Headphone out)

Digital

Analog



Audio moat is transparent and width 40mil



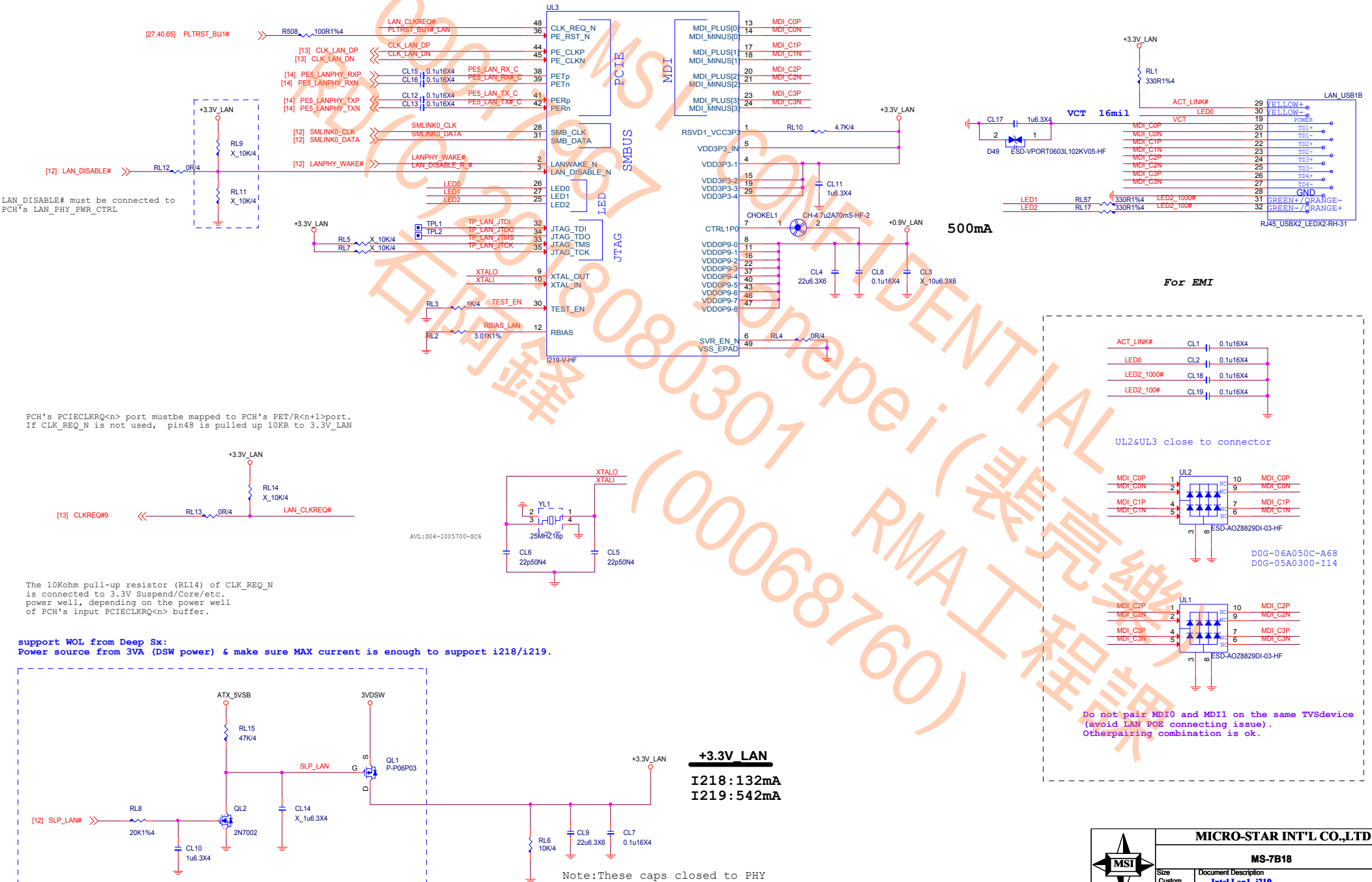
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00017967 jonepei (裴亮樂)  
RD(C)2018080301 RMA工程課  
石阿鋒 (00068760)



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Intel Lan- i211

The diagram illustrates the pin configuration for the i211 module, showing connections for various pins and components. The module is labeled "i211" in the center.

**Pin Connections:**

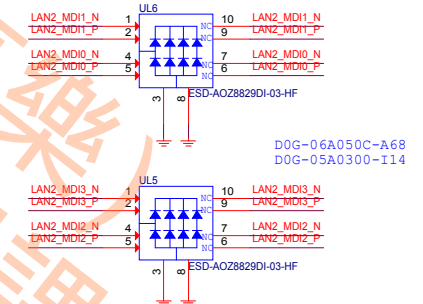
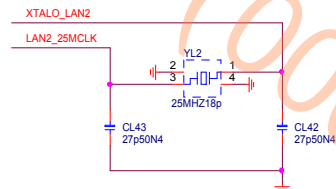
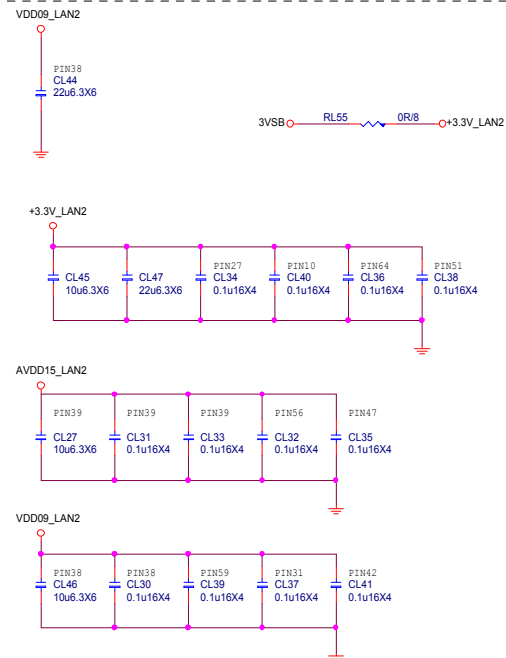
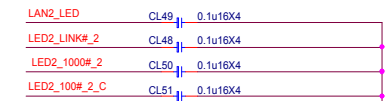
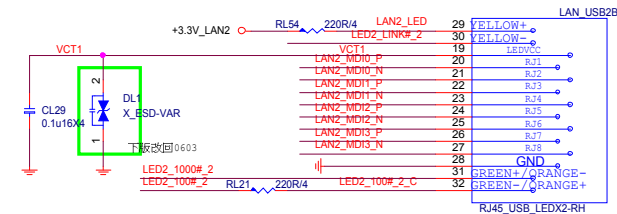
- CLK\_I211\_DP** (Pin 13) to **CLK\_I211\_DN** (Pin 13)
- PE4\_I211\_TXP** (Pin 14) to **PE4\_I211\_TXN** (Pin 14)
- PE4\_I211\_TXN** (Pin 14) to **PE4\_I211\_RXP** (Pin 14)
- PE4\_I211\_RXP** (Pin 14) to **PE4\_I211\_RXN** (Pin 14)
- PLTRST\_BU#** (Pin 27, 39, 65) to **PCH\_WAKE#** (Pin 12, 19, 20, 22, 24, 25)
- R122** (100R1%4) to **PLTRST\_BU#** (Pin 12, 19, 20, 22, 24, 25)
- 3.3V\_LAN2** to **RL38** (10K/4) and **RL37** (10K/4)
- 3.3V\_LAN2** to **RL49** (10K/4)
- 3.3V\_LAN2** to **RL19** (10K/4) and **RL20** (10K/4)
- 3.3V\_LAN2** to **RL51** (10K/4) and **RL53** (10K/4)
- LED2\_100#\_2** (Pin 31) to **LED2\_LINK#\_2** (Pin 30) and **LED2\_1000#\_2** (Pin 33)
- LED2\_1000#\_2** (Pin 33) to **LED2** (Pin 33)
- LAN\_PWR\_GOOD** (Pin 1) to **DEV\_OFF\_N** (Pin 28)
- LAN\_PWR\_GOOD** (Pin 1) to **LAN\_PWR\_GOOD** (Pin 1)
- NC** (Pin 22) to **GND** (Pin 65)

**Component Values:**

- R122**: 100R1%4
- RL38**: 10K/4
- RL37**: 10K/4
- RL49**: 10K/4
- RL19**: 10K/4
- RL20**: 10K/4
- RL51**: 10K/4
- RL53**: 10K/4

**Module Labels:**

- i211**
- WGI211AT-SLJXZ-SLJXY-HF**



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HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

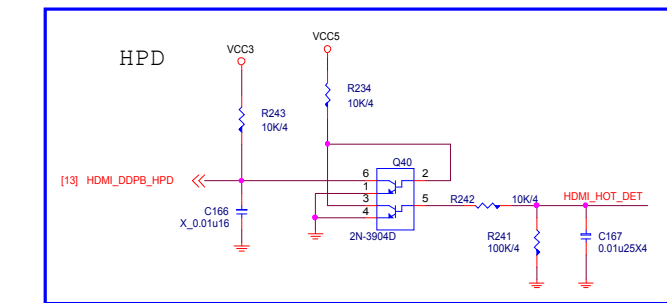
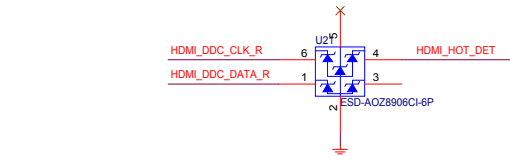
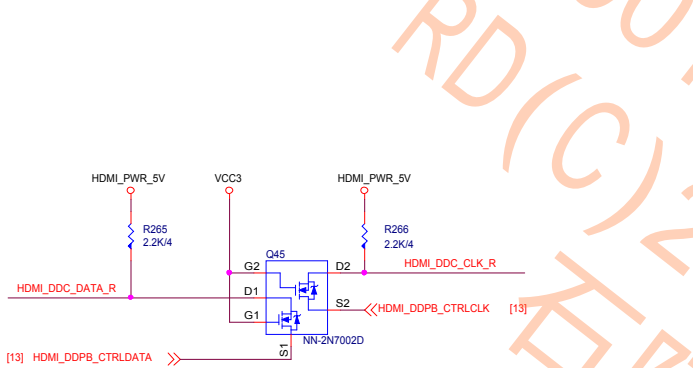
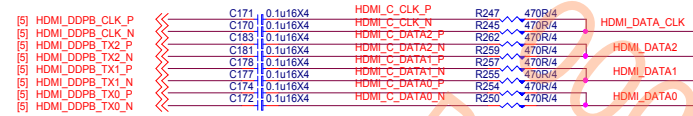
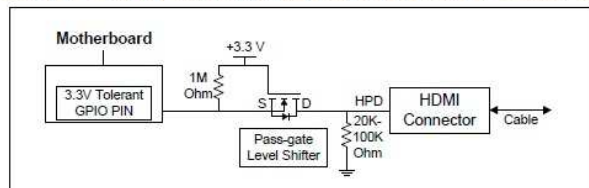
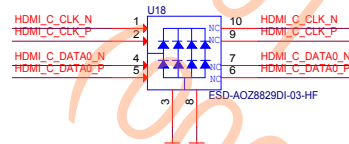
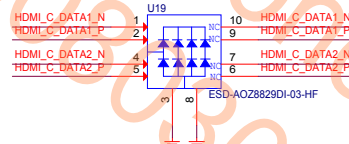
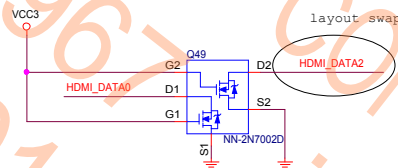
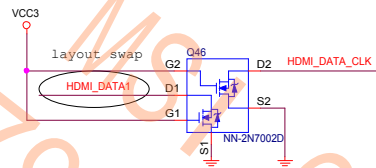


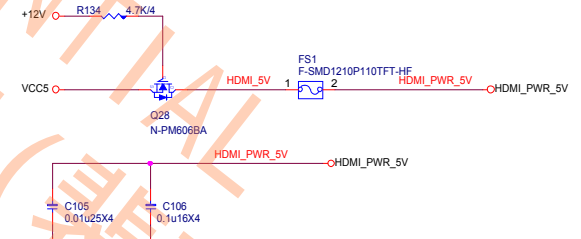
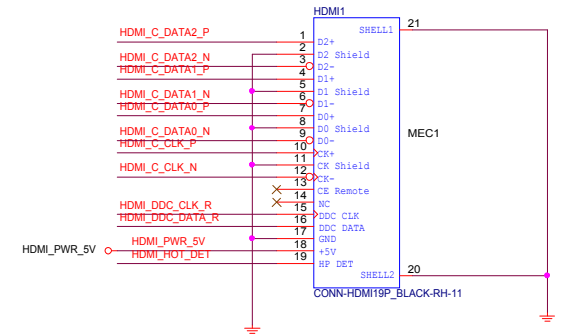
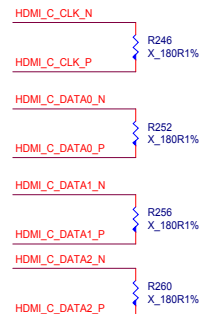
Figure 7-9. HDMI 1.4\* HPD Cost Reduced Level Shifter Design Recommendation



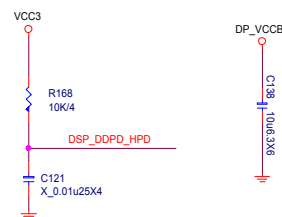
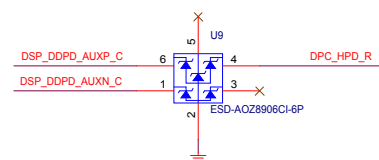
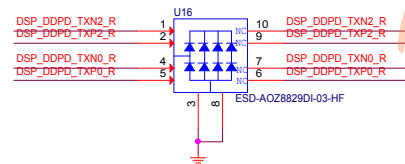
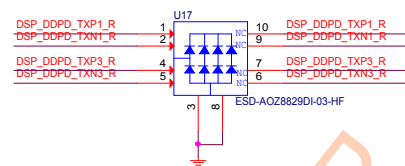
Note: 3.3V transistor gate supply must turn off when CPU power is turned off.



For EMI







DP\_VCCB trace don't less than 30 mil

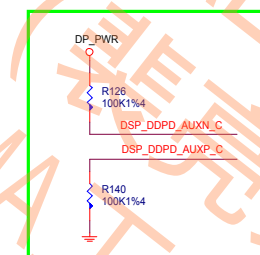
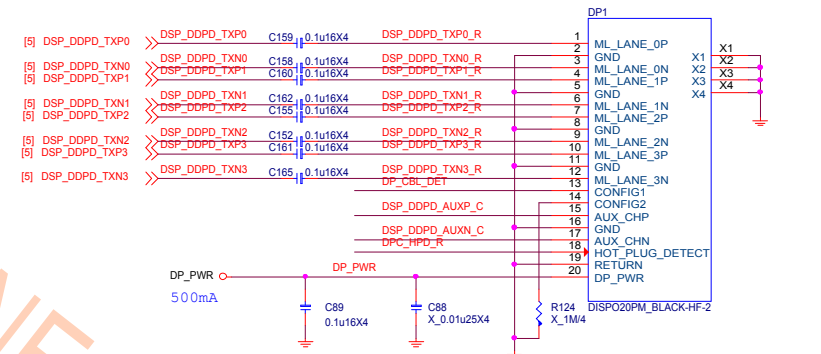
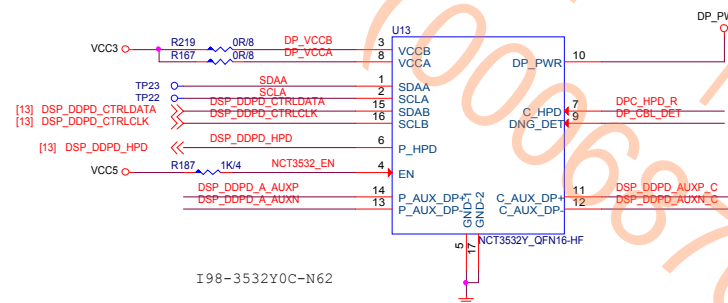
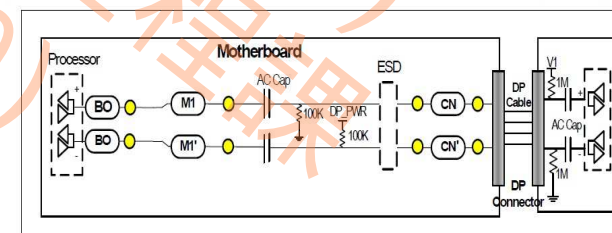
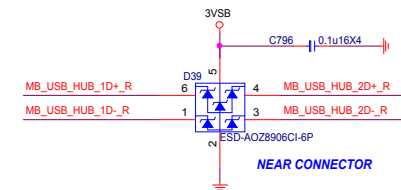
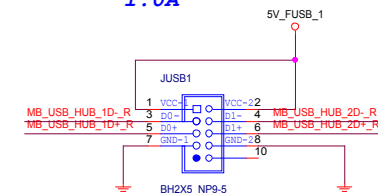


Figure 5-6. DT and AIOCFL DisplayPort\* Auxiliary Channel External (Topology A)

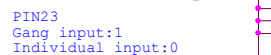




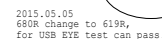
$1.0A$



4-port at high-speed mode. --> 58.6mA

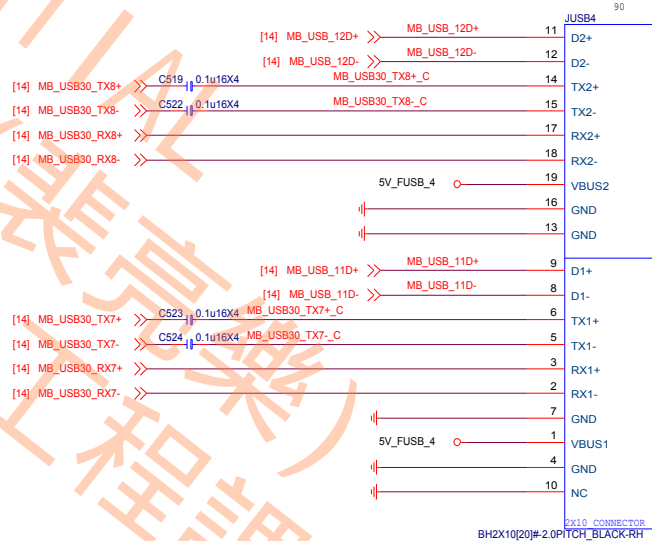
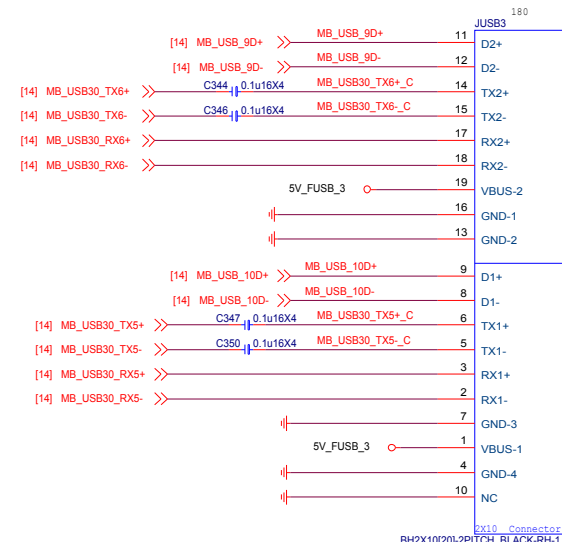
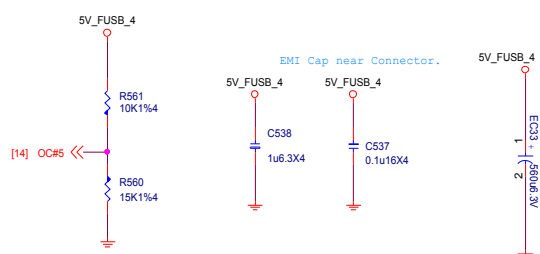
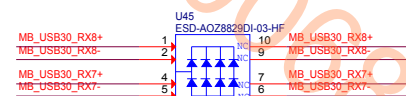
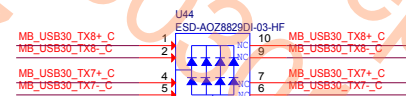
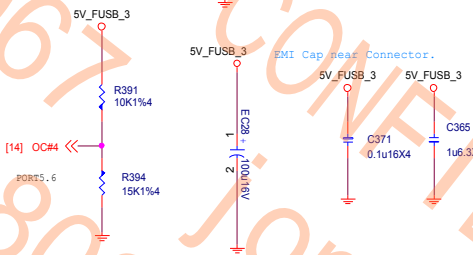
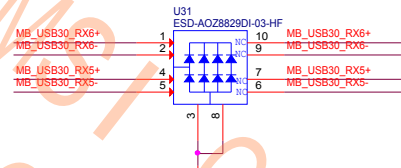
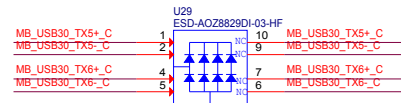
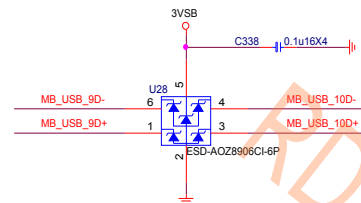


```
PIN22
0: GL850G-50 is bus-powered
1: GL850G-50 is self-powered
```

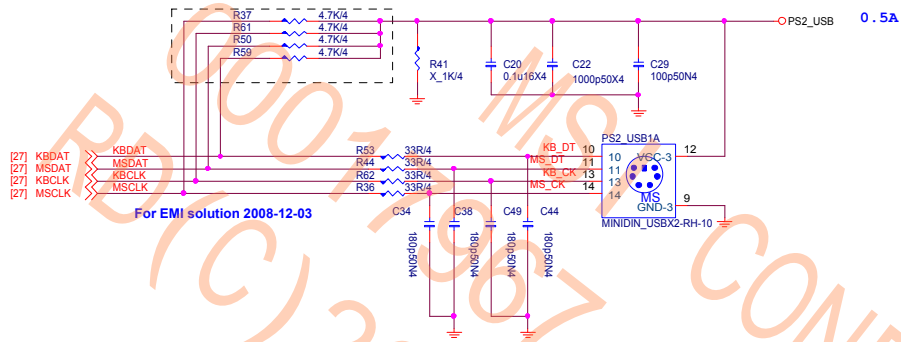
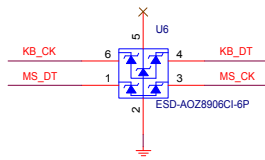


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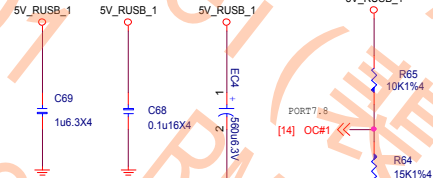
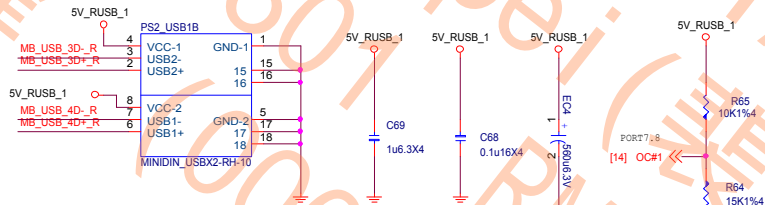
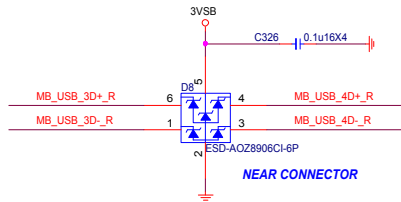
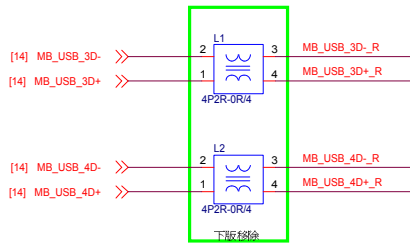
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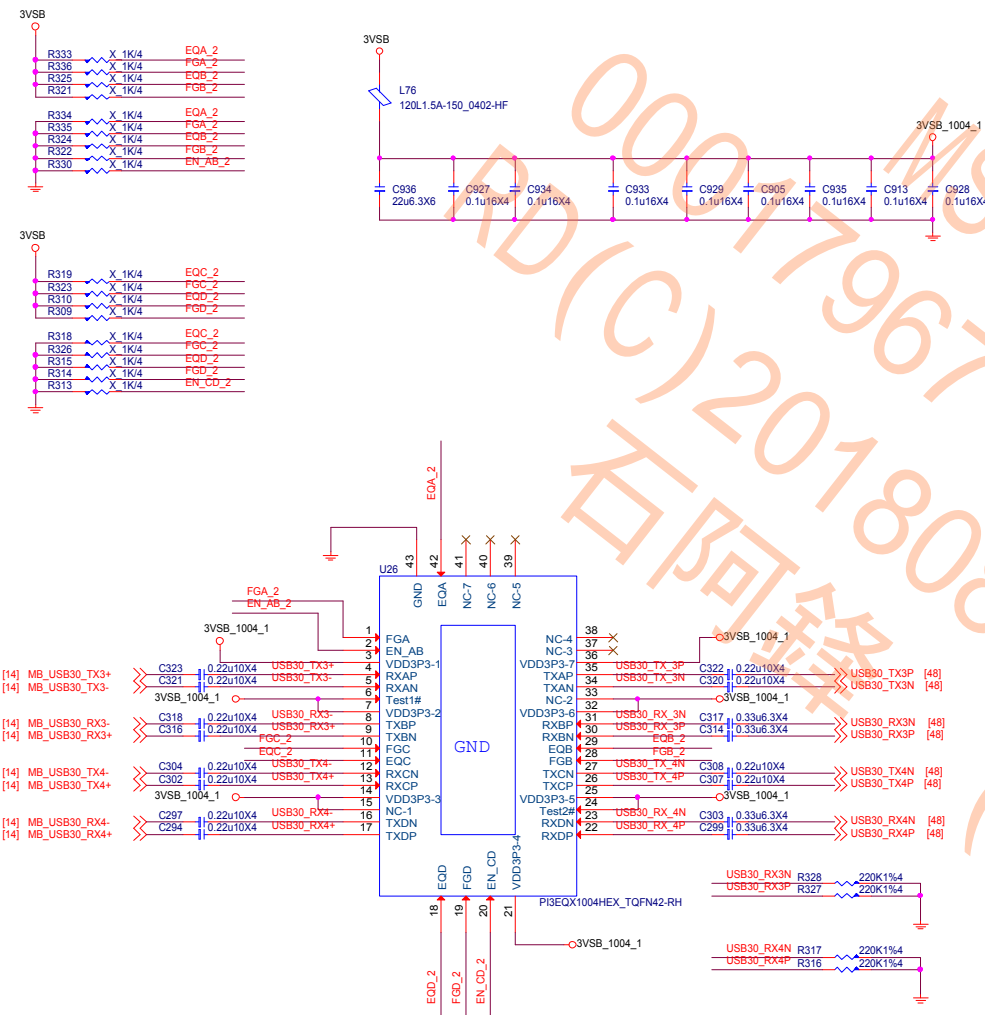
PS2 KEYBOARD & MOUSE CONNECTOR



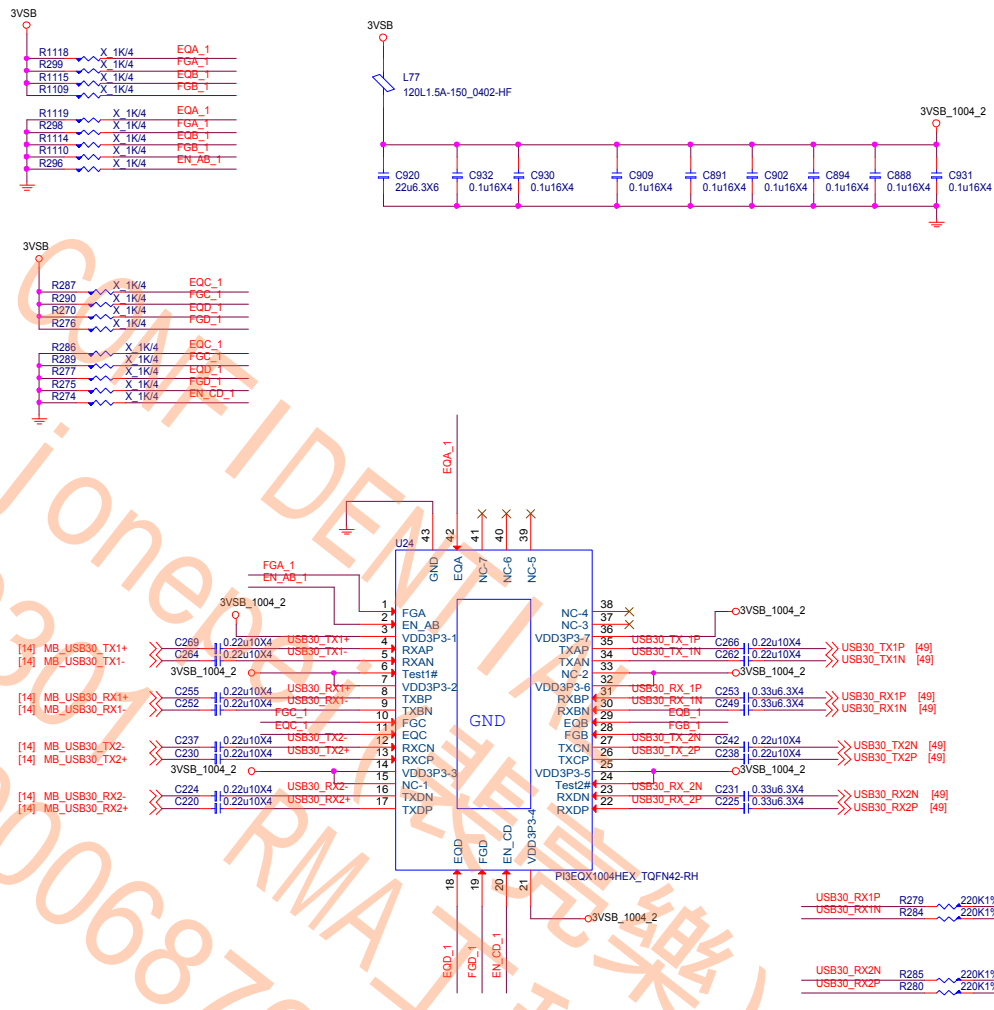
PS2-USB



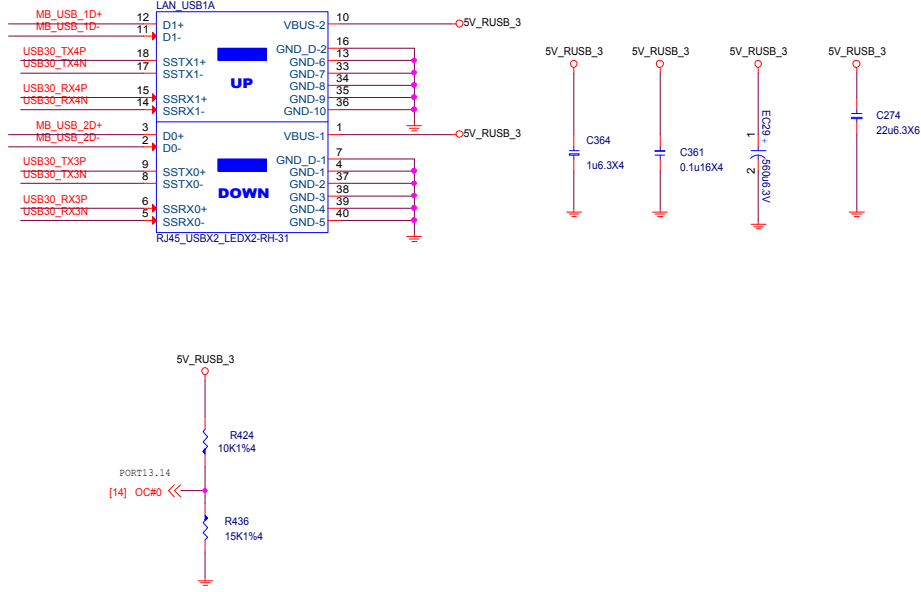
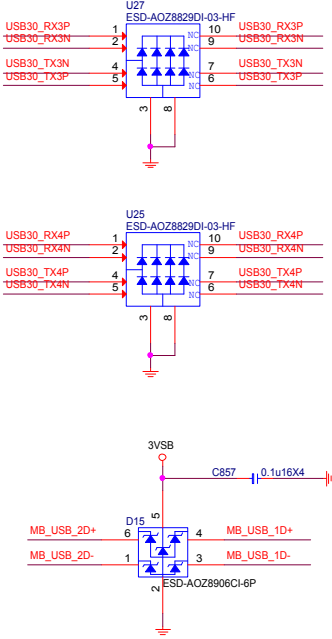
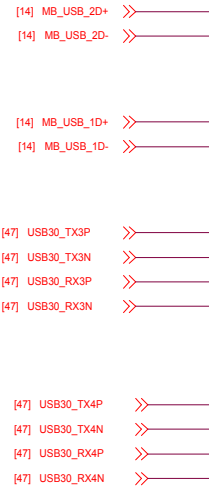
# Rear USB3.1 Redriver



# Rear USB3.1 Redriver



LAN1 USB2.0 &3.0

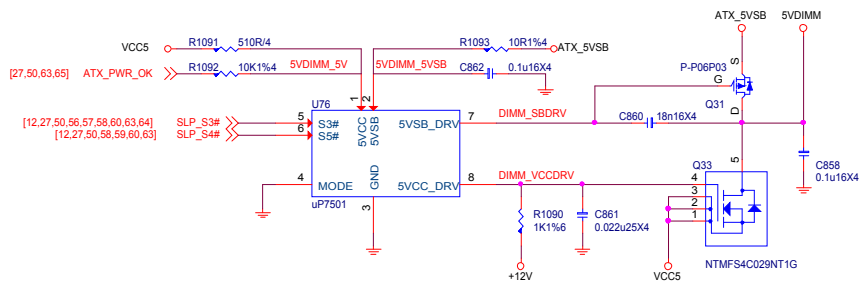






## 5VDIMM FOR DDR

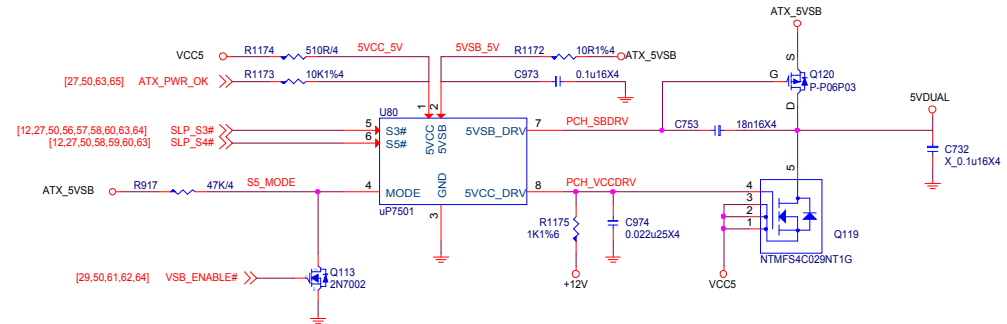
4.8A



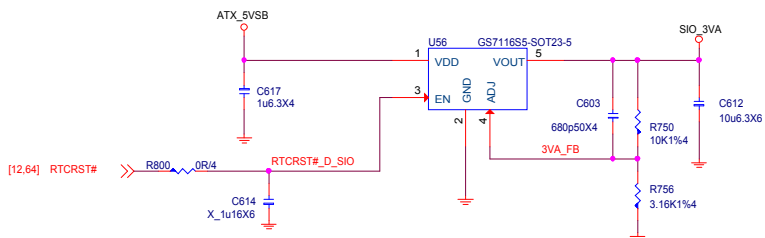
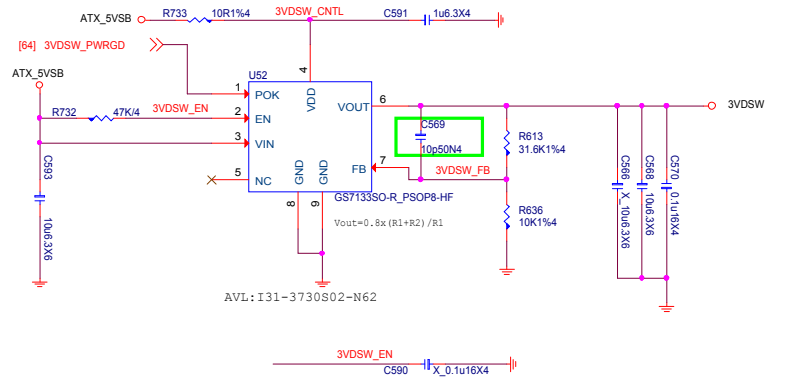
```
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3
```

## 5VDUAL

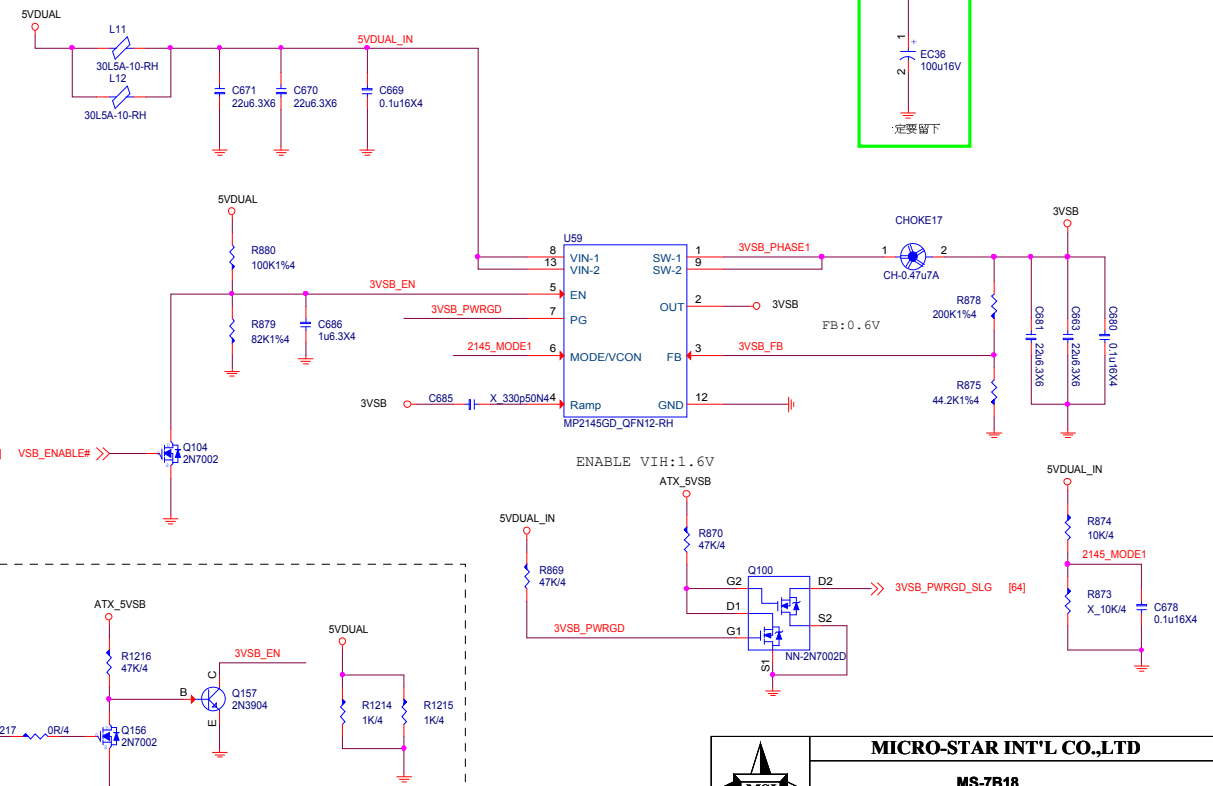
6.25A



## 3VDSW 0.512A



3VSB cost down 4.7A

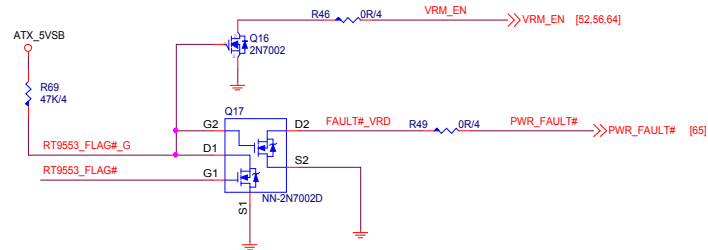
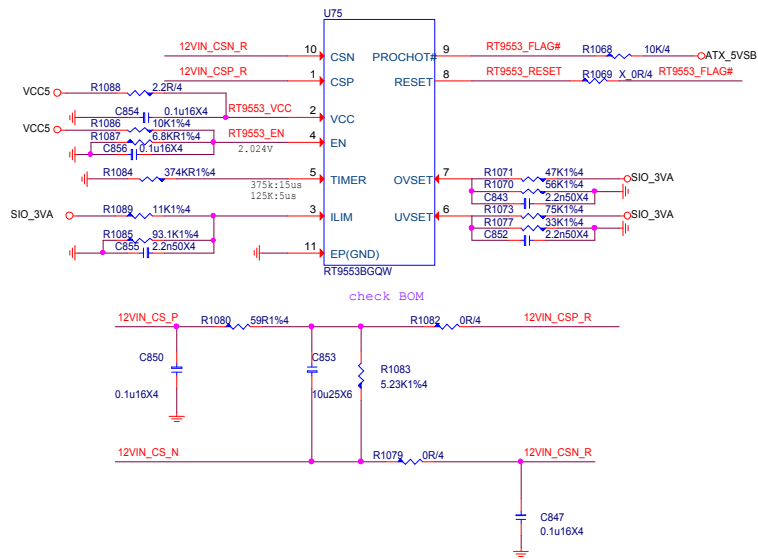


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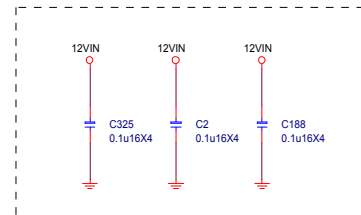
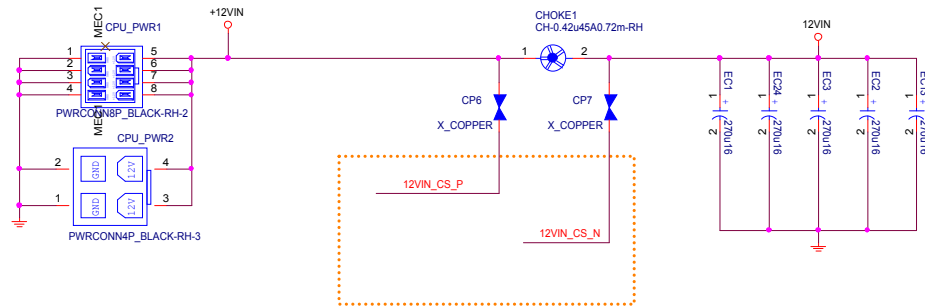
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for S5-G3 3VSB\_EN ISSUE



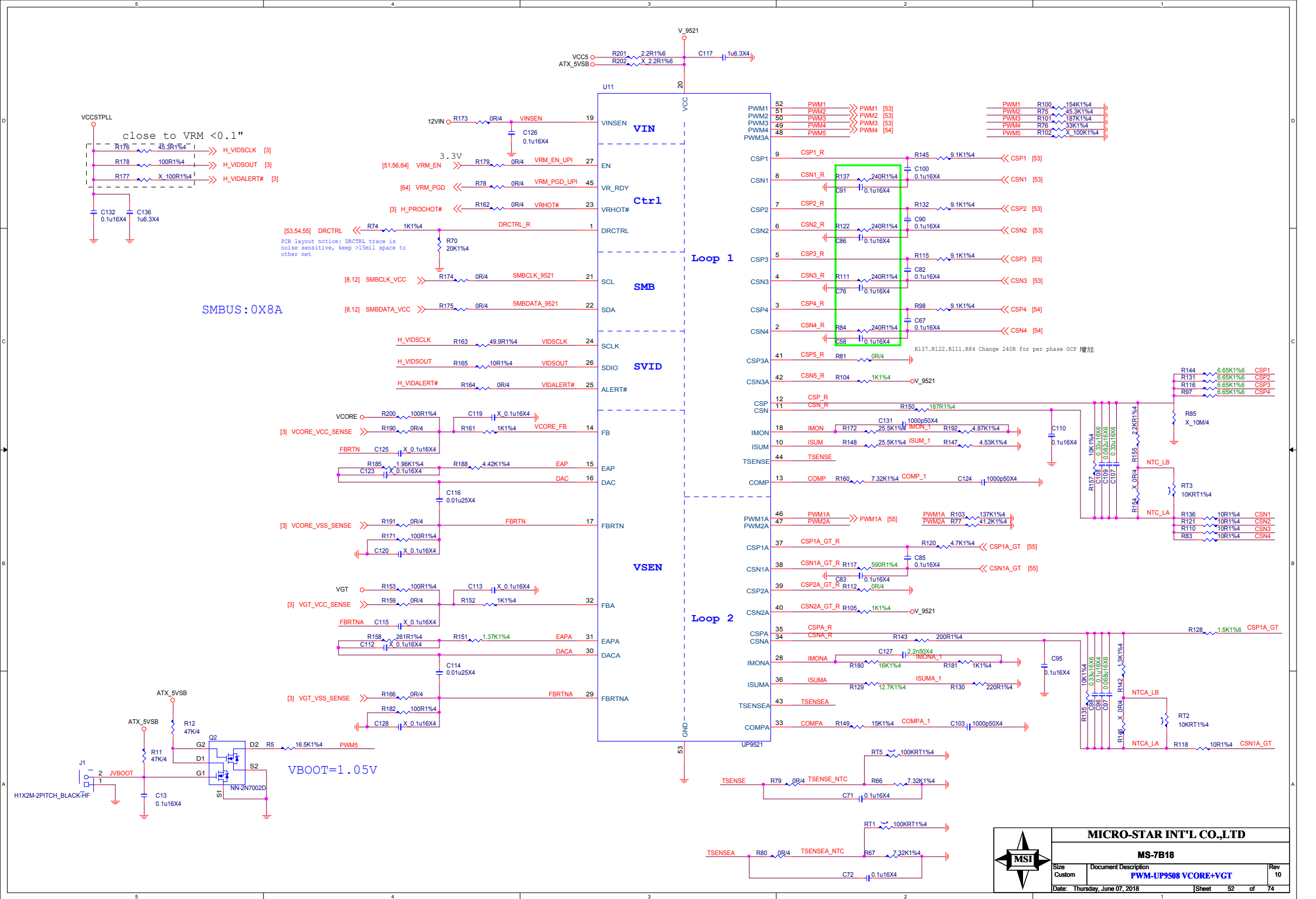
OCp : 34A\*1.3=44.2A  
Real OCp : ??A

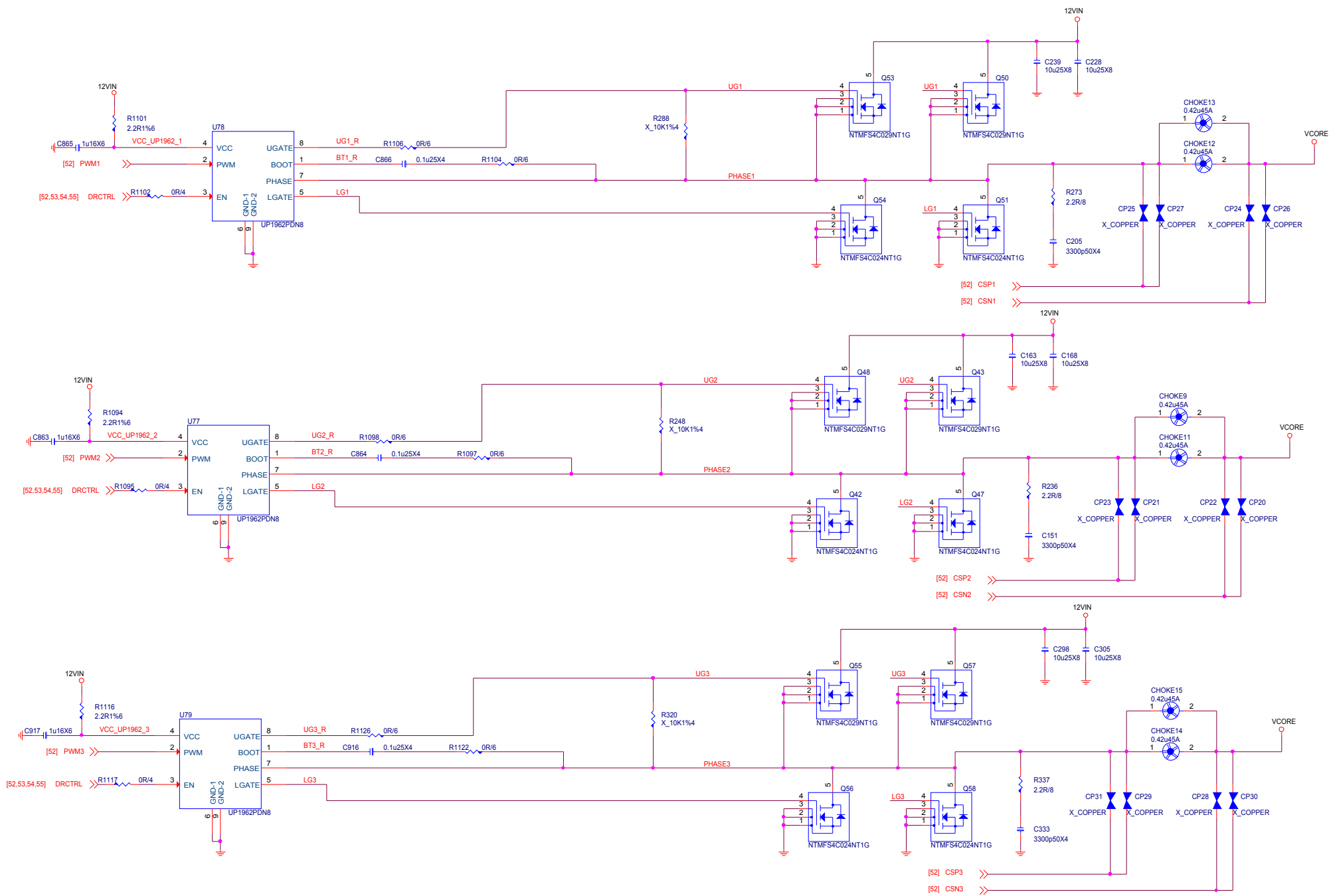


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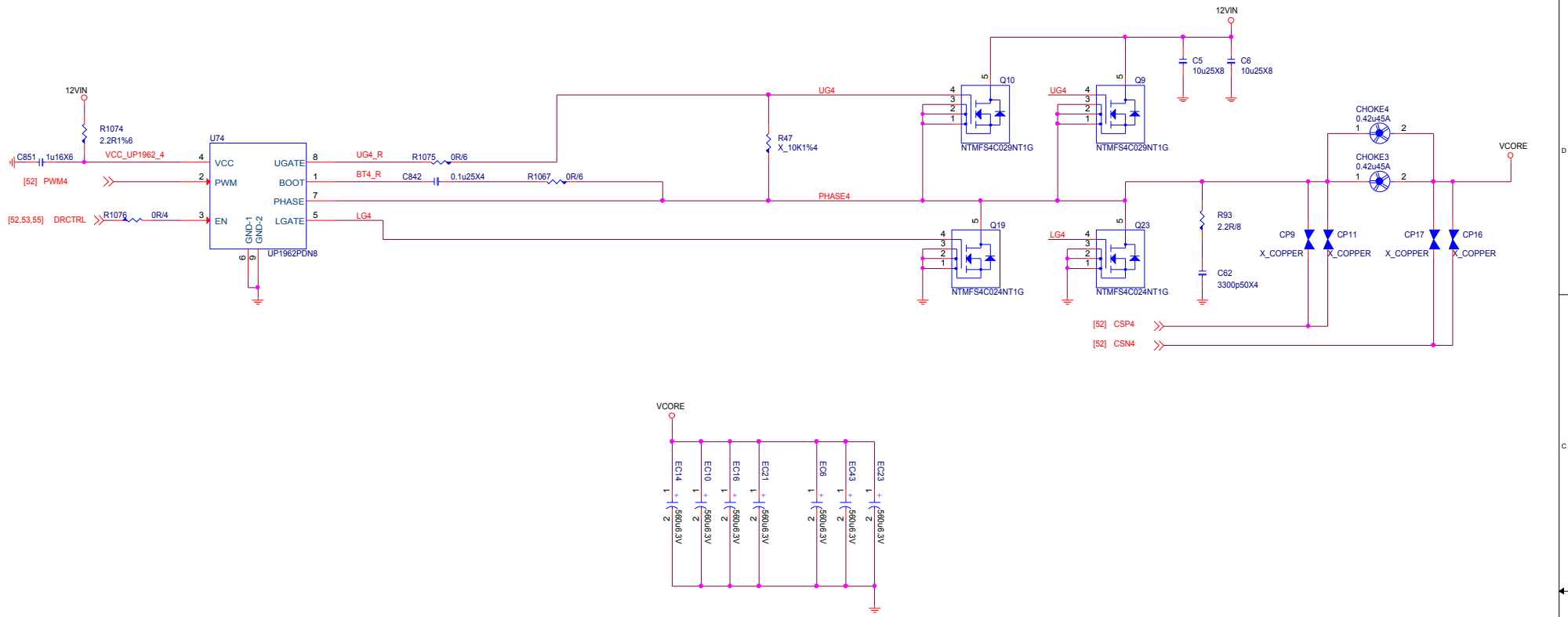


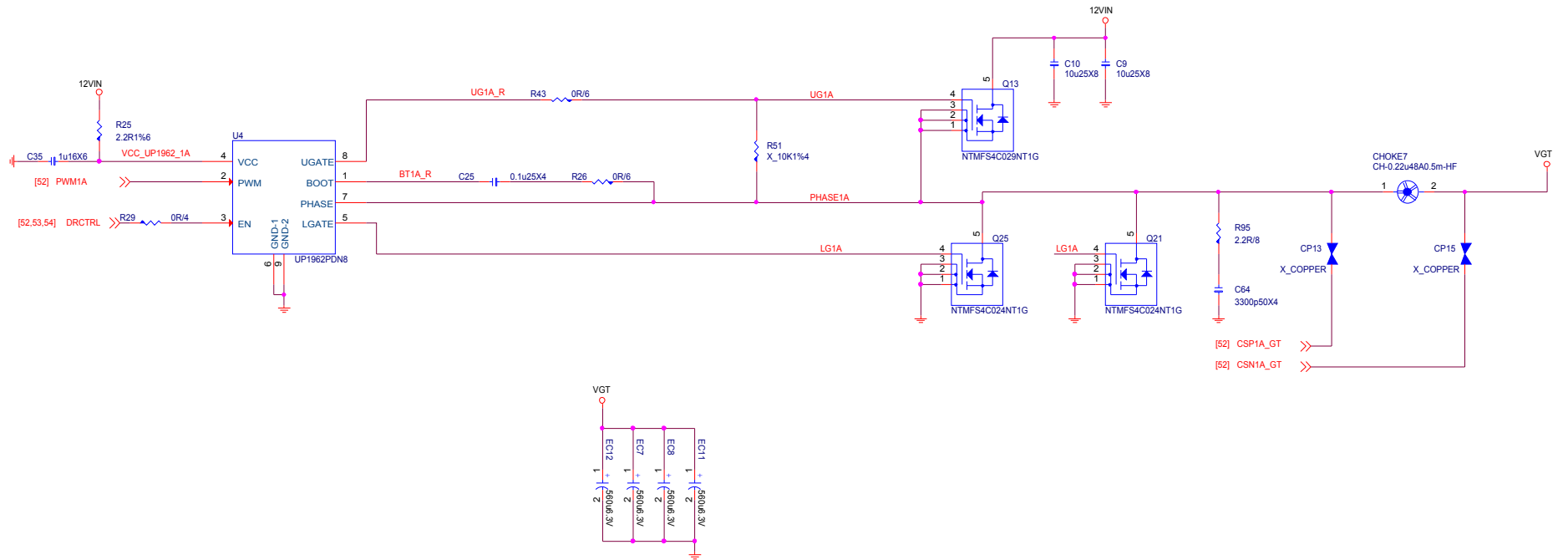


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# SA Power:1.05V,11.1A

OCP:14.43A

Rocset =  $1.3 * I_{max} * R_{dson(10V)} / I_{ocset}$   
 =  $14.43 * 2.8\text{mohm} / 10\mu\text{A}$   
 = 4.04K

Rdson(10V) 10V

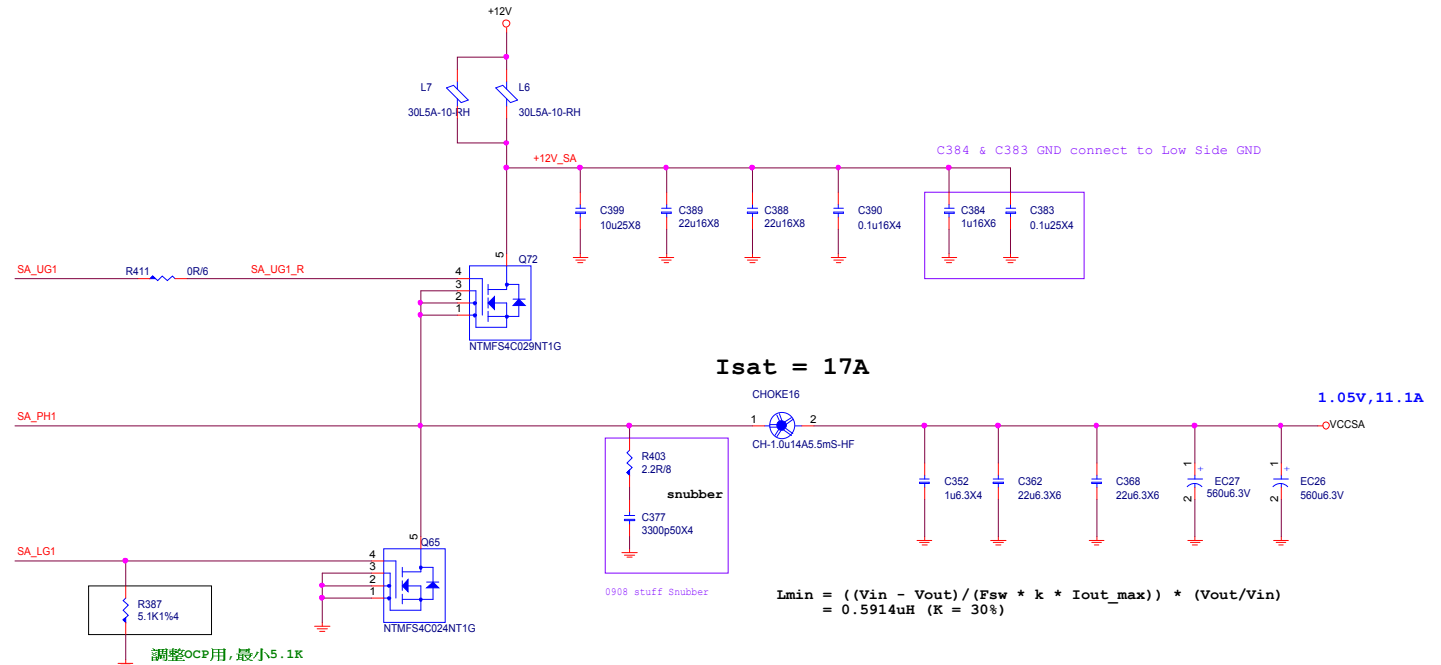
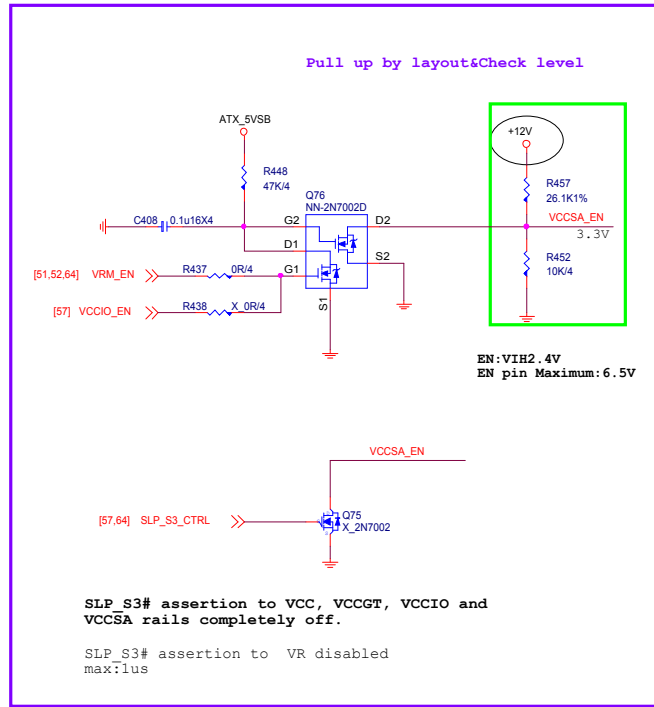
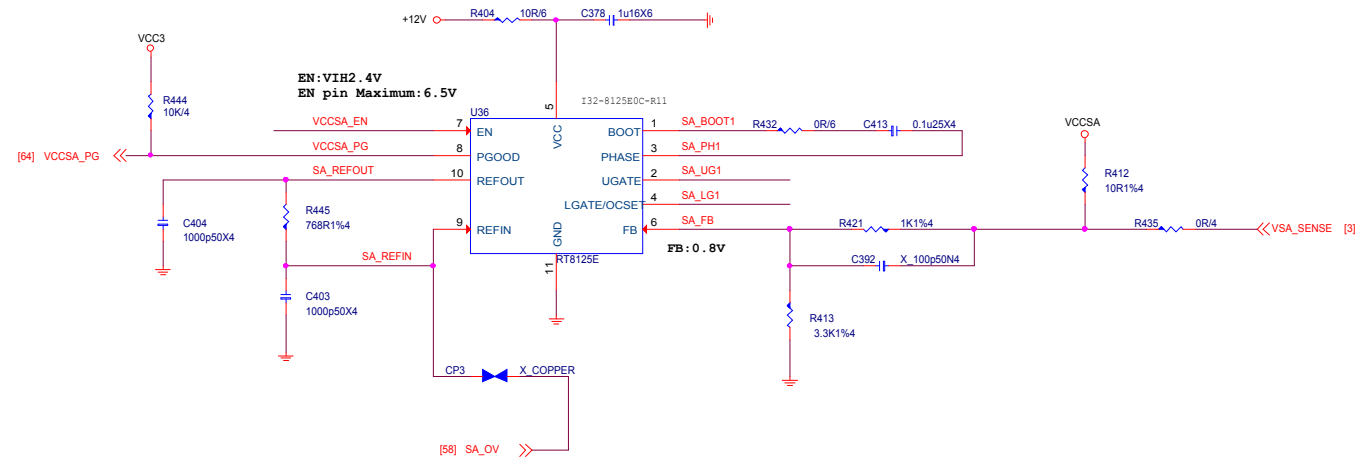
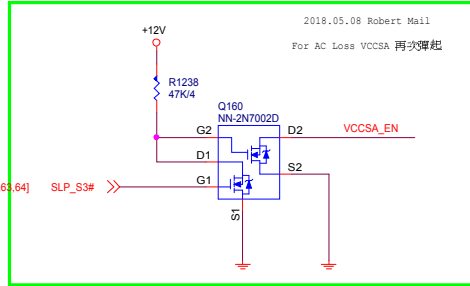
MOS : 2.8mohm

最低5.1K

D03-4C02403-005

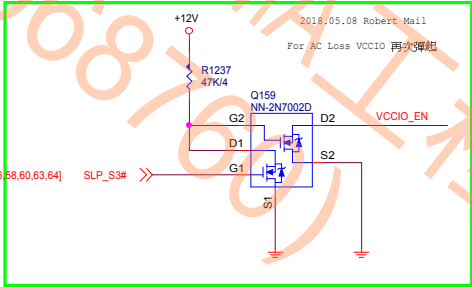
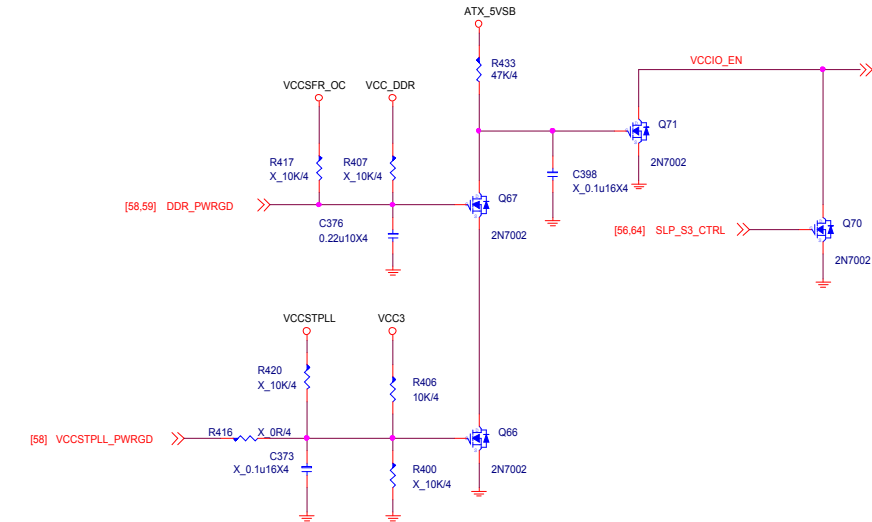
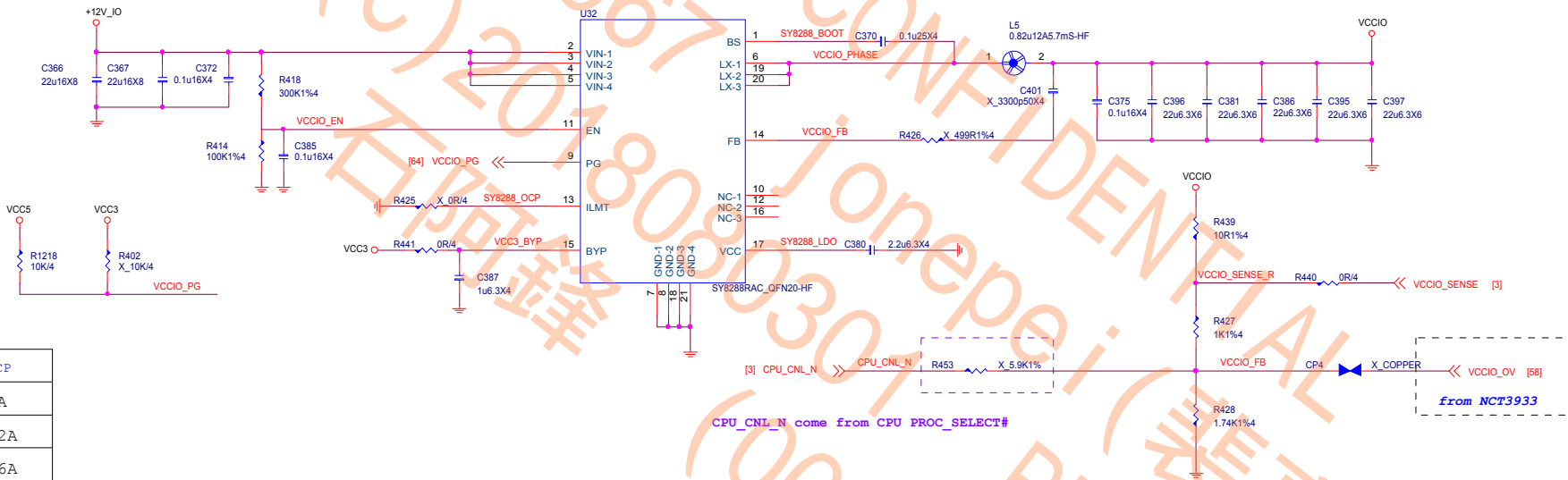
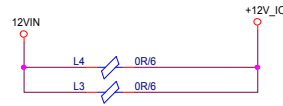
Current limit=  $5.1K * 10\mu\text{A} / 2.3\text{mohm}$  = 22.17A

Current limit=  $5.1K * 10\mu\text{A} / 2.8\text{mohm}$  = 18.21A

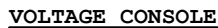


IO Power:0.95V,6.4A

IMAX 10A  
ILIMIT=10A~12A  
IOC=ILIMIT+40%\*IMAX/2=12A~14A.



1.05V; 230mA



ATX\_5VSB ATX\_5VSB

R466 10K1%4

C448 0.1u16X4

R465 X 1K/4

[12,58,66] SMBCLK\_VSB [12,58,66] SMBDATA\_VSB

U39

1 VCC

2 ADD\_SEL

4 SCL

5 SDA

3 GND

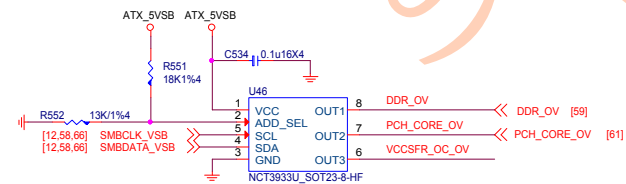
8 OUT1 SA\_OV

7 OUT2 VCCIO\_OV

6 OUT3 VCCSTPLL\_OV

NCT933U, SOT23-6HF

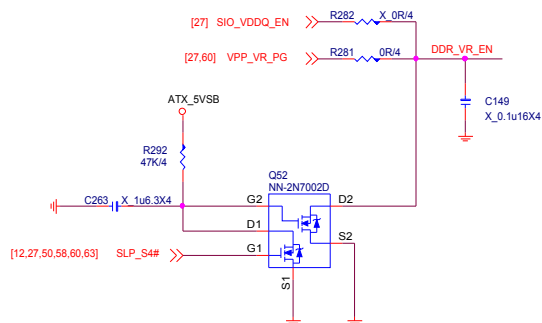
1.2V; 130mA



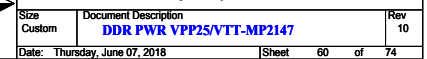
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Current limit=  $10K \cdot 10\mu A / 3.3mohm = 30.3A$   
Current limit=  $10K \cdot 10\mu A / 4mohm = 25A$

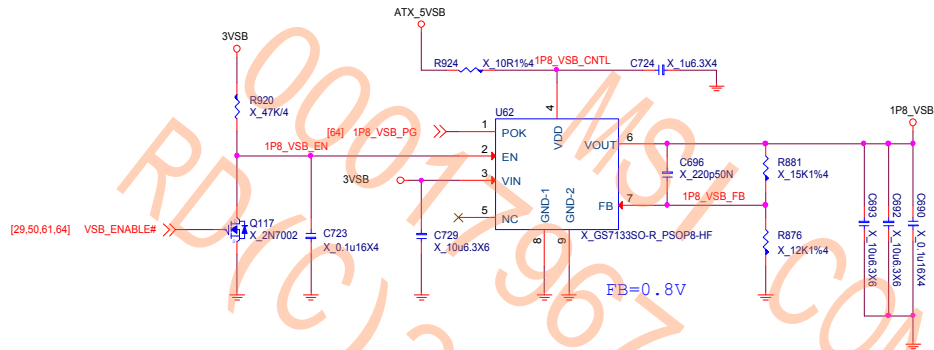
[illegible]

**OCP:7.5A**



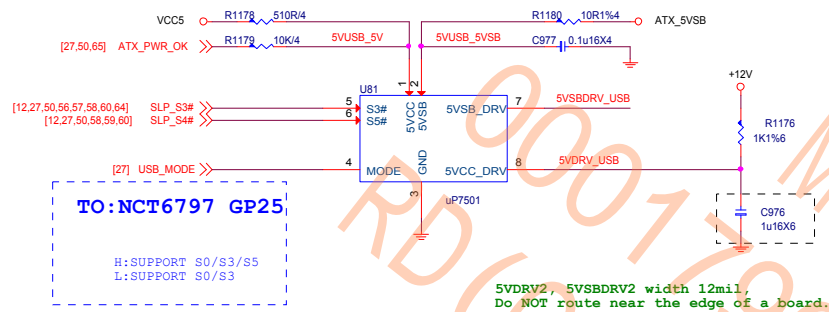


1P8\_VSB

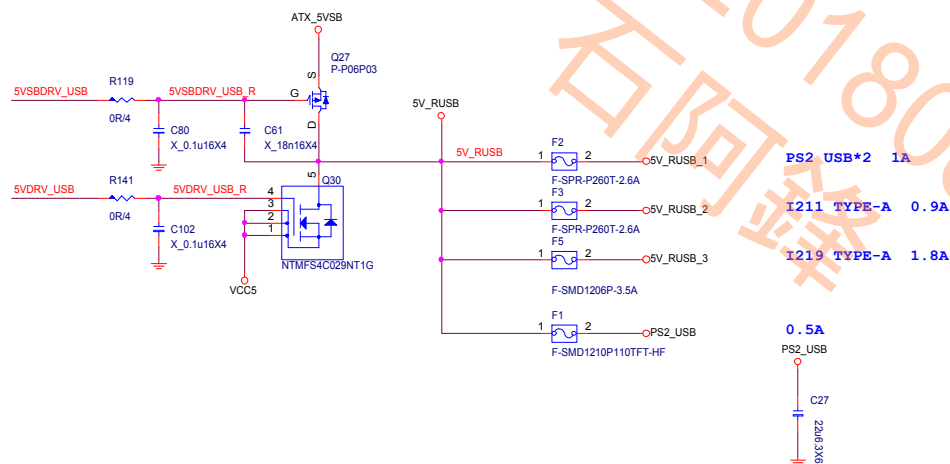




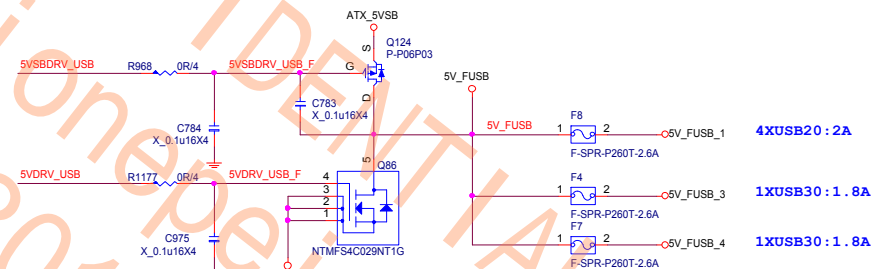
## USB POWER



## REAR USB PORT POWER



## FRONT USB PORT POWER



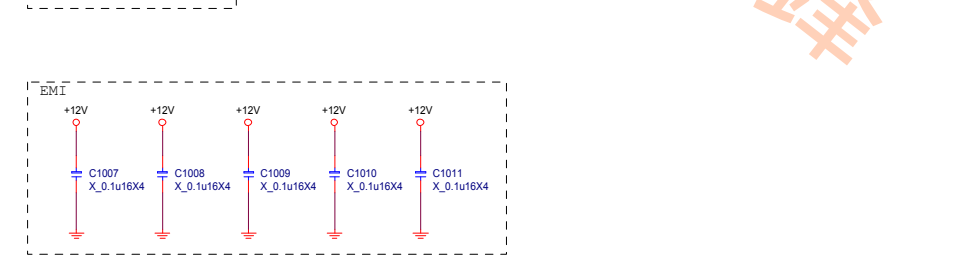
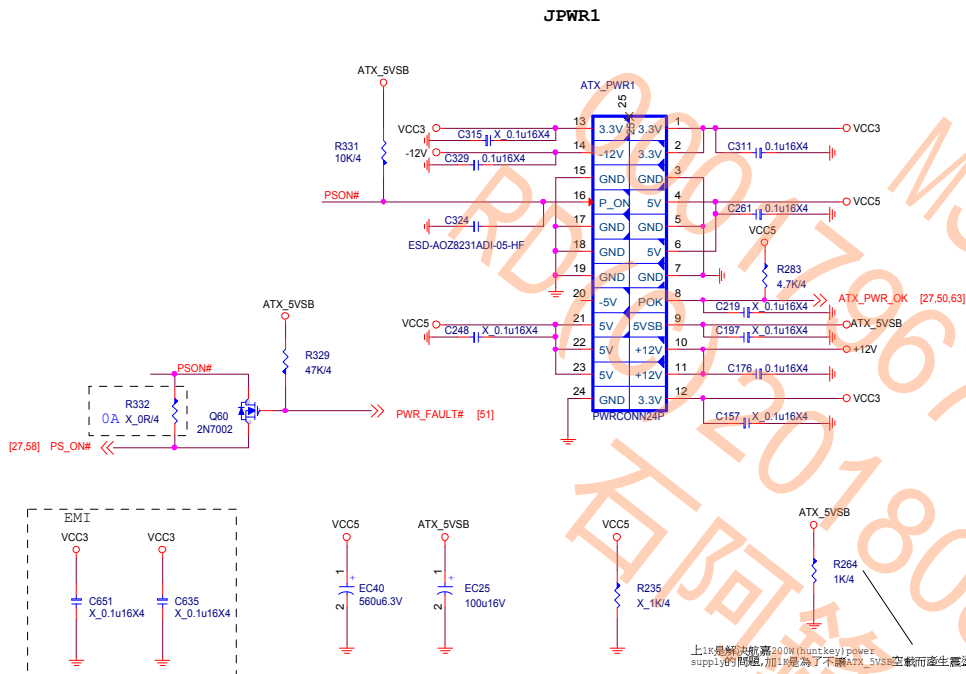
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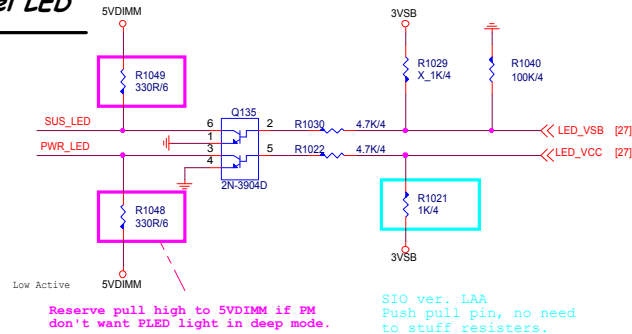
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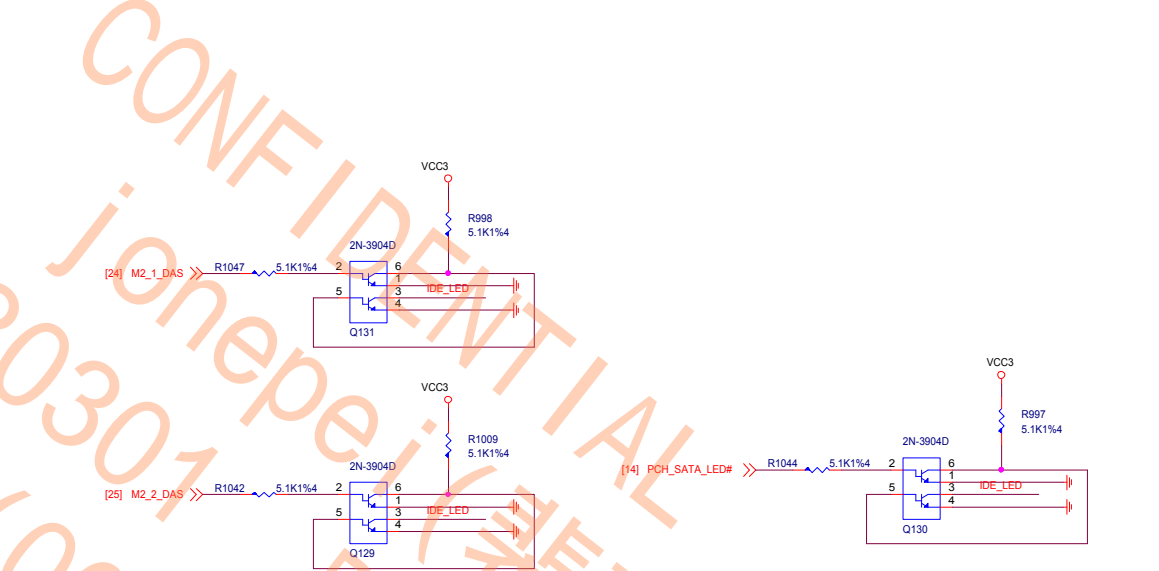
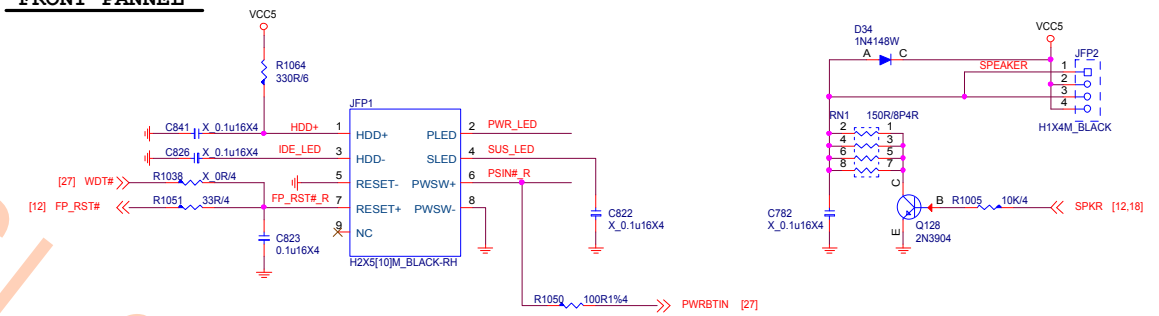
## ATX POWER CONNECTOR



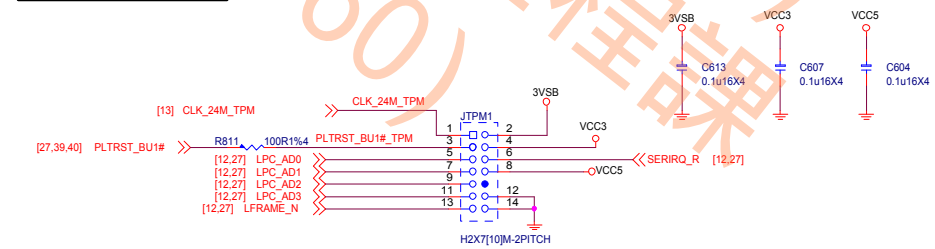
## Front Panel LED



## FRONT PANNEL

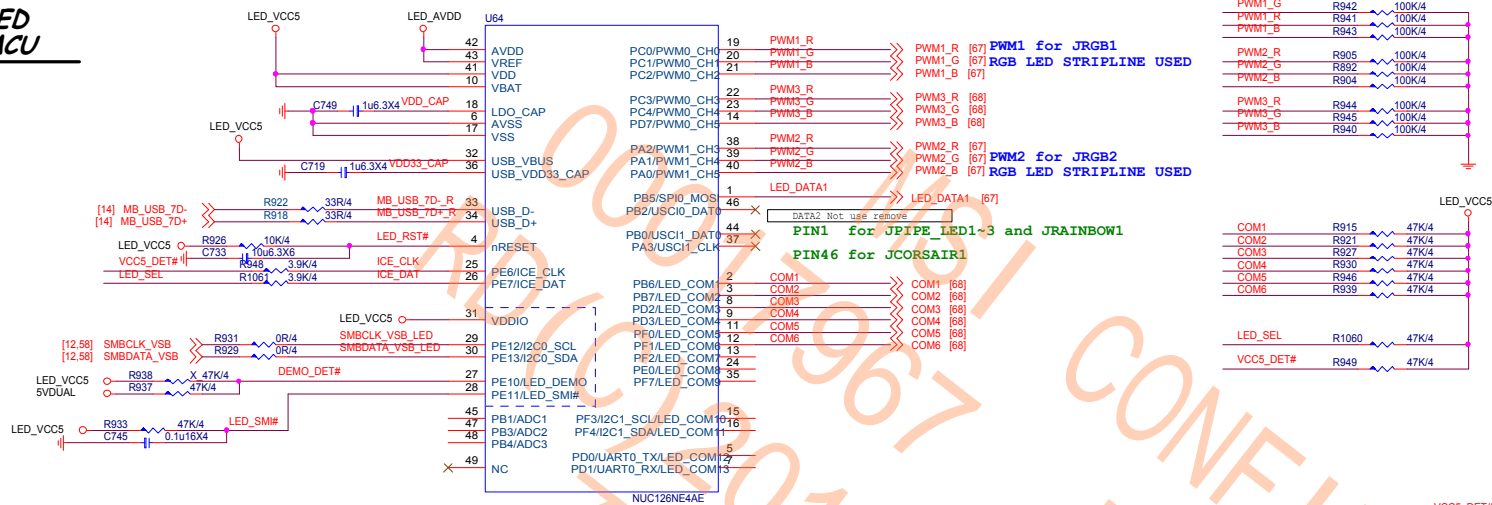


## TPM Pin Header

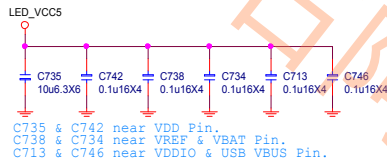
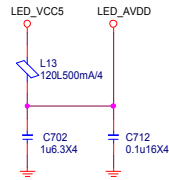


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# LED MCU



C702 & C712 near AVDD Pin.



C735 & C742 near VDD Pin.  
C738 & C734 near VREF & VBAT Pin.  
C713 & C746 near VDDIO & USB VBUS Pin.

If SPEC has LED demo function without demo button, DEMO\_DET# must pull up to LED VCC5, Q319 need to stuff and control by LED\_VCC5\_EN. PS. R2069 remove, R2032 and Q319 need to stuff

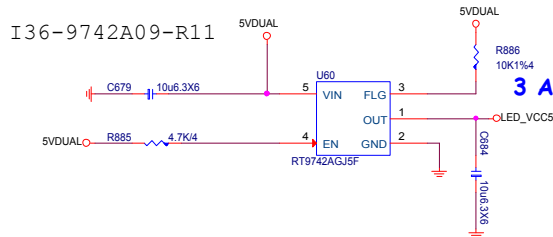
## EXTERNAL POWER INPUT

7B18 Not use remove

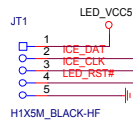
## External Power

7B18 Not use remove

## JT1 for FW update



For FW update.



## Voltage HW monitor

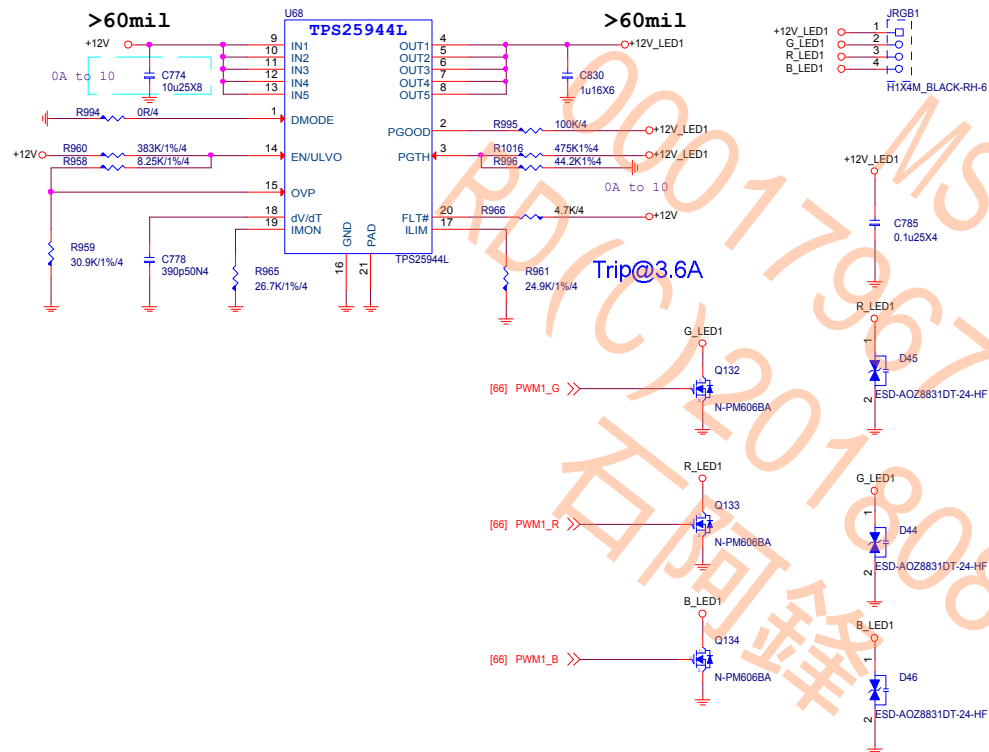
7B18 Not use remove



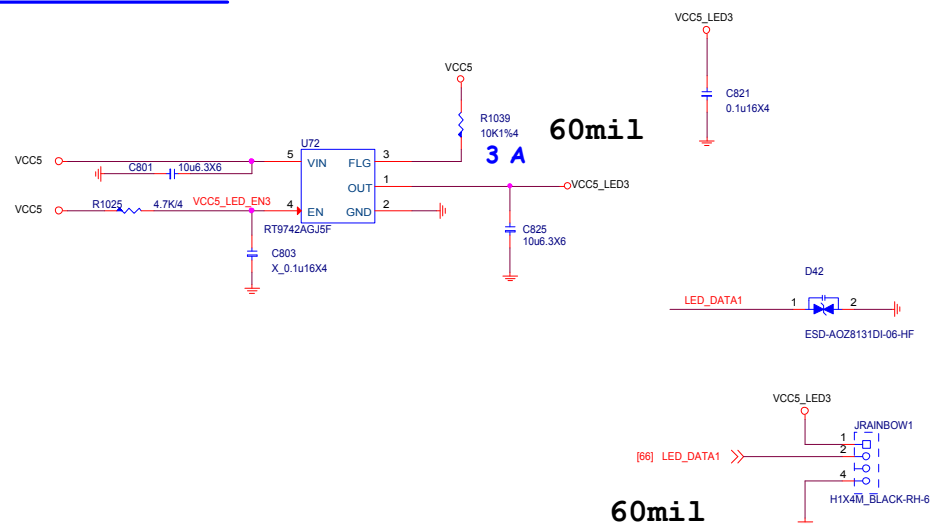
MICRO-STAR INT'L CO.,LTD

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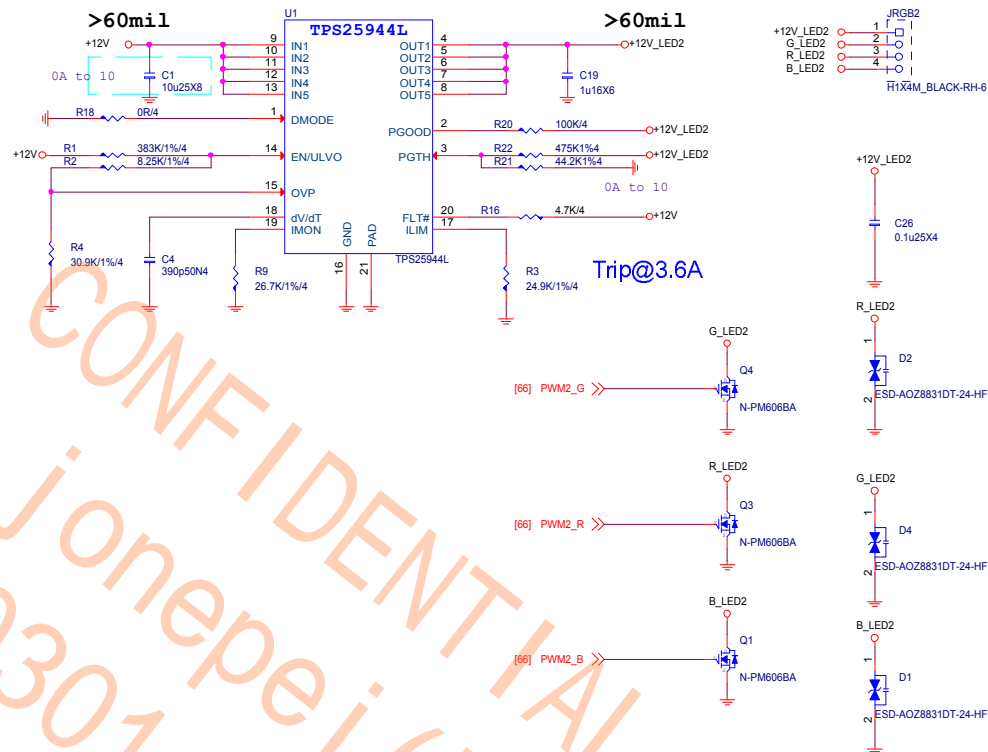
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JRGB1

**LED STRIPLINE  
JRAINBOW1**



JRGB2



JCORSAIR1

7B18 Not use remove



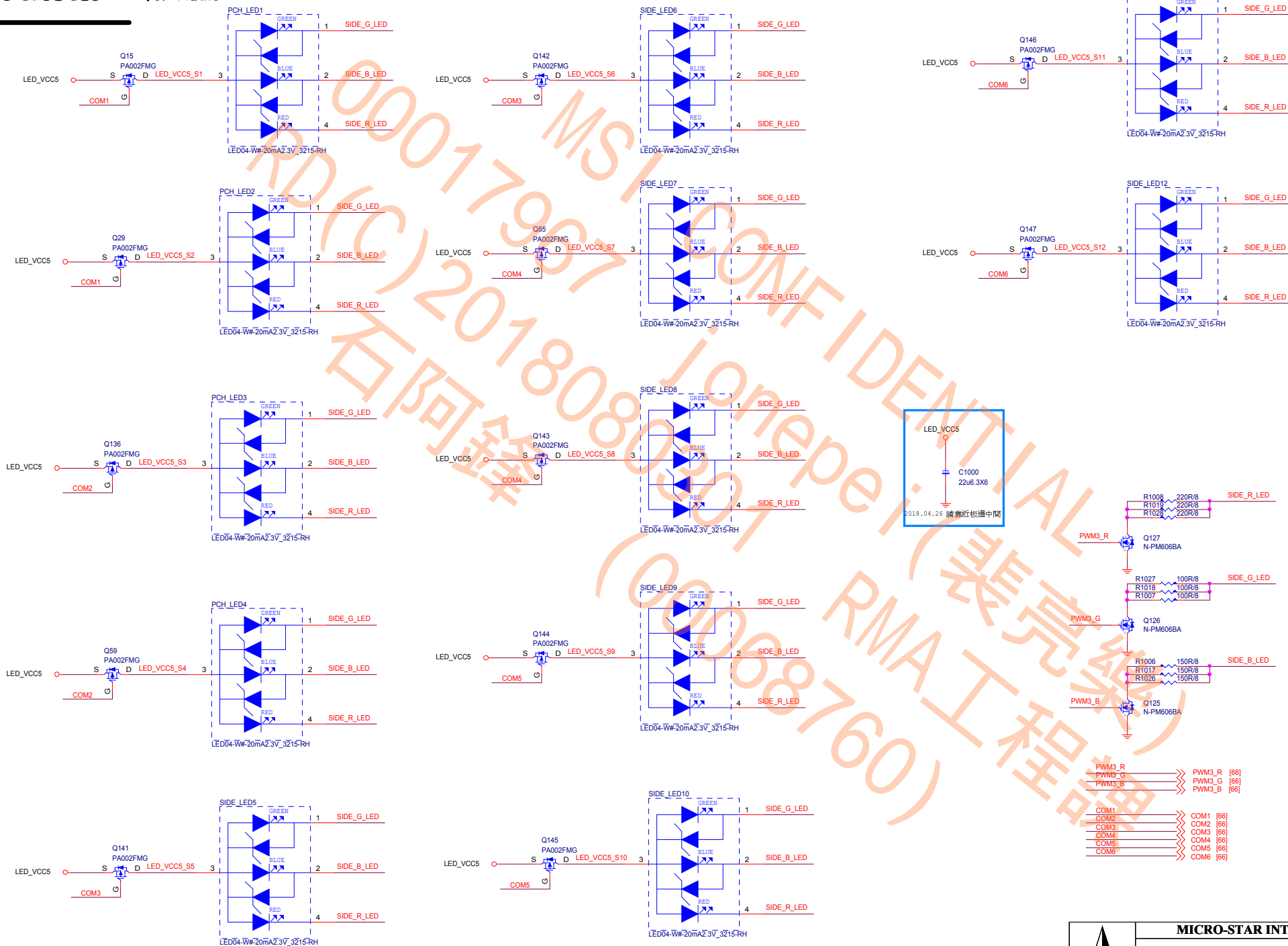
**MICRO-STAR INT'L CO.,LTD**

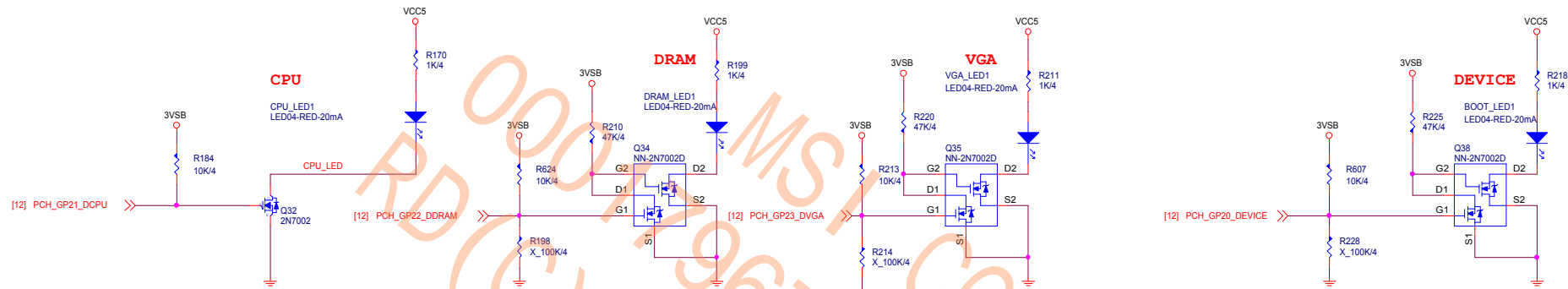
**MS-7B18**

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Custom	<b>EMI CAP</b>	10

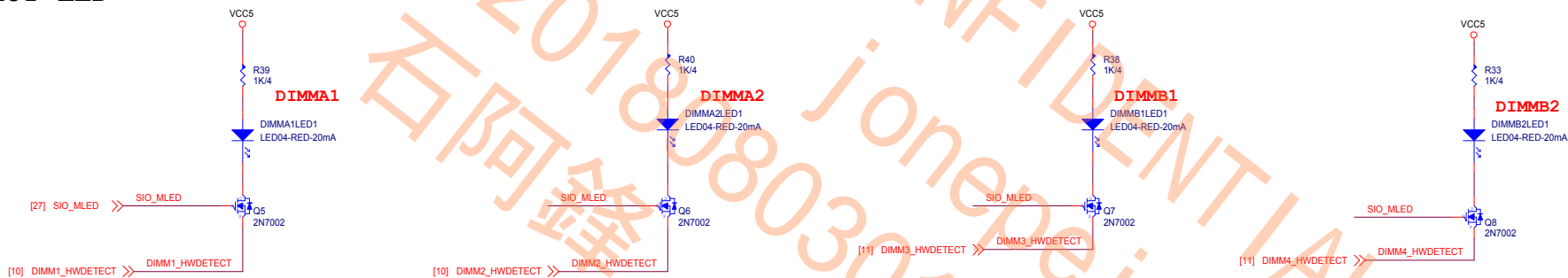
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# BOARD SIDE LED \*12 for Audio

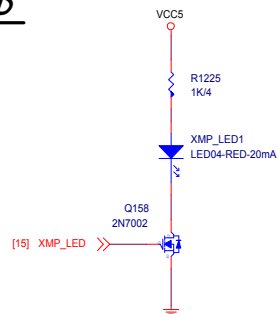




## DIMM SLOT LED



## XMP LED



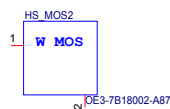
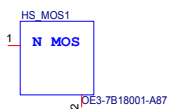




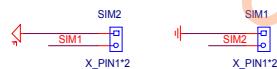
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PD0-07B1810-G37



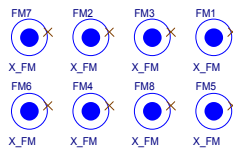
## HEATSINK



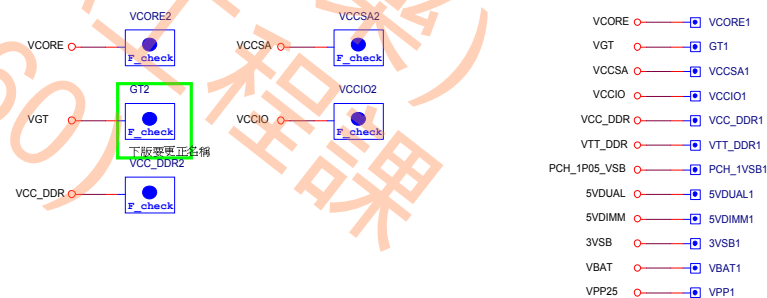
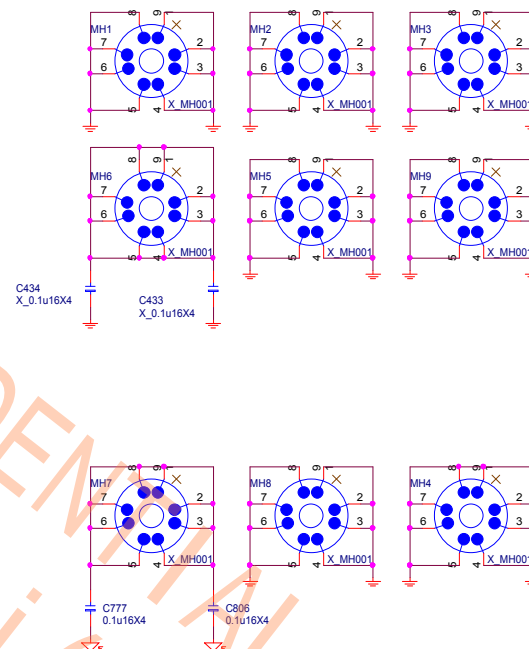
## Simulation



## Optical Fiducial Marks-120



## Mounting Holes



MICRO-STAR INT'L CO.,LTD

MS-7B18

Size	Document Description	Rev
Custom	Manual Parts	10
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